Linearity Optimization of DG MOSFETs for RF Applications

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Abstract

RF linearity of double-gate MOSFETs is investigated using accurate two-dimensional simulations. The linearity has been analyzed using the Talyor series. Transconductance is dominant nonlinear source of CMOS. It is shown that DG-MOSFET linearity can be improved by a careful optimization of channel thickness, gate oxide thickness, gate length, overlap length and channel doping concentration. The minimum P_{IP3} data are compared in each case. It is shown that DG-MOSFET linearity can be improved by a careful optimization of channel thickness, gate oxide thickness, gate length, overlap length and channel doping concentration..

I. Introduction

Double-Gate (DG) MOSFETs have been widely recognized as suitable candidates for use in future CMOS ultralarge-scale integrated circuits at sub-50-nm scale [1]. High linearity is an essential requirement in integrated CMOS RF systems, which ensures that high order harmonics and inter-modulation terms are negligible at the output. Although there are system level techniques to improve linearity, they all require complex circuit [4]. A transistor-level linearization is more appropriate for the power amplifiers in portable system, which requires an analysis of linearity behavior at device level as a function of important design parameters. For a direct evaluation of RF linearity performance of MOSFETs, drain saturation current, I_{DSAT}, or threshold voltage, V_T, are not suitable figures of merit in the way they are used in digital circuits. A reliable metric used to evaluate linearity efficiency of each MOSFETs is the input-referred IP3 point [4]. For a matched input resistance of R_s=50Ω, P_{IP3} can be expressed in terms of Taylor expansion coefficients [8]:

$$P_{IP3} = \frac{2g_{m1}}{3g_{m3}R_s} = \frac{4(\frac{\partial I_d}{\partial V_g})}{R_s(\frac{\partial^3 I_d}{\partial V_g^3})} \quad (1)$$

Besides transconductance, other important transfer parameters of MOSFETs, such as the output conductance g_d also have a dependence on the operation point as well as frequency, hence introduce further nonlinearities. However, due to the comparatively low value (50Ω) of the output resistance, the influence from the output conductance can be ignored according to the results by reported by [5].

II. Deviced Simulations

Fig. 1 shows the 2-D schematic view of double-gate MOSFET used for 2-dimensional device simulations. The device has gate length 30 nm (L_{gate}), 1 nm gate oxide (T_{ox}), 8 nm silicon body thickness (T_{Si}) as shown in Fig. 1. Although traditionally compact models are used for linearity analysis, such approximations are either totally inadequate or currently non-existent for RF performance evaluation of sub-50 nm MOSFETs with complex channel-gate charge coupling features. The use of physics-based device simulator provides a more complete and accurate analysis alternative. To investigate the linearity performance as well as dc characteristics of DG-MOSFET, the SILVACO device simulator was used

[6]. Advanced models were used in the device simulator ATLAS. Simulated dc transfer characteristics are generated using a very small step size for the gate voltage. The I_d-V_g characteristics were used to obtain transconductance (g_{m1}) and its second derivative (g_{m3}), which are then substituted into (1) for the calculation of input level P_{IP3}. All the Taylor-series parameters are extracted from the dc I_d-V_g curve of the model. g_{m1}, g_{m2}, and g_{m3} versus V_{gs} are shown for a constant V_{ds}(=1.2V) in Fig. 2.

In simulations various drain bias from 0.1 V to 1.5 V was used, but we use the data at 1.2 V of drain bias generally. To examine the influence of gate length scaling, we also performed simulations with 20, 25, 35, 40, 50 and 60 nm gate length. And gate oxide thickness is changed variously. Another simulation were performed with 1.5, 2, 2.5 and 3 nm gate oxide to know effect of oxide thickness on linearity performance. To investigate silicon body thickness dependence, silicon body thickness also was changed from 6 nm to 14 nm varionsly.

To evaluate effect of channel doping concentration on linearity performance of DG-MOSFET, channel doping concentration decreases from initial concentration (N_a = 10^{18} cm^{-3}) to 10^{15} cm^{-3} gradually. And we controlled doping profile of donor in order to change overlapped length between gate and Source/Drain region extends. So we could find which is more advantaged between overlapped structure and non-overlapped structure from linearity performance point of view.

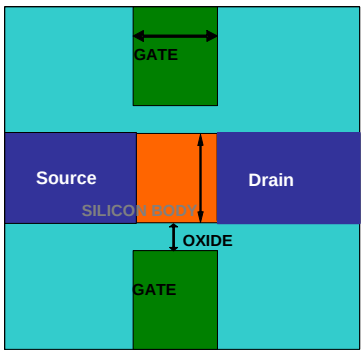

Fig. 1. General Double Gate MOSFET structure

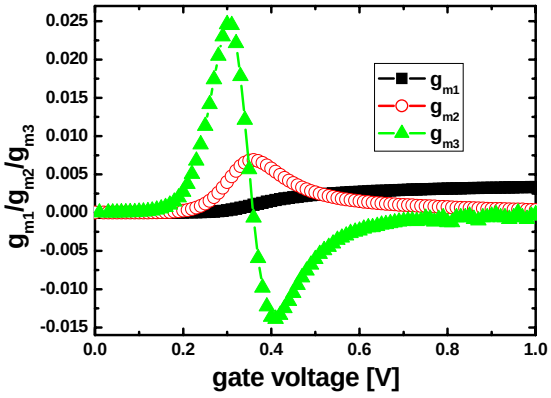

Fig. 2. Double Gate MOSFET transconductance

III. Results

To investigate the channel length dependence, the effective gate length of the devices is scaled from 60 nm down to 20 nm, while keeping all other parameters the same. We find that the linearity performance of DG MOSFETs degrades gradually as the gate length is reduced as while increasing at the case of very short channel length shown in Fig. 3.

The silicon body scaling has a small impact on the linearity of DG-MOSFETs as shown in Fig. 4. Linearity of DG-MOSFET decreases steadily down to 6 nm body thickness. This implies that a DG-MOSFET designed for RF performance may require a thicker body than those for digital applications.

Fig. 5. shows gate oxide thickness vs. linearity performance. With decreasing gate oxide thickness, the minimum P_{IP3} decreases gradually. So too thin gate oxide may have disadvantage in device scaling.

P_{IP3} slightly increases with channel doping N_A in Fig. 6. Linearity of DG-MOSFET is almost constant before doping concentration grows N_a = 10^{16} cm^{-3} while P_{IP3} slightly increases as channel doping concentration is increase from N_a = 10^{17} cm^{-3} to N_a = 10^{18} cm^{-3}.So to speak, as too low acceptor concentration has disadvantage in linearity, a little channel doping is necessary to ensure stable linearity.

We changed overlap length by controlling donor doping in source and drain region. Simulations of nine

devices which have various overlap length from -4 nm to 4 nm were performed. As the overlapped length between gate and Source/Drain region extends, linearity performance improves as shown in Fig. 7. It has a significant drop of the minimum P_{IP3} between 0 nm underlap and 1 nm underlap. So a device of structure which has some overlapped region between gate and S/D operates with a better linearity performance.

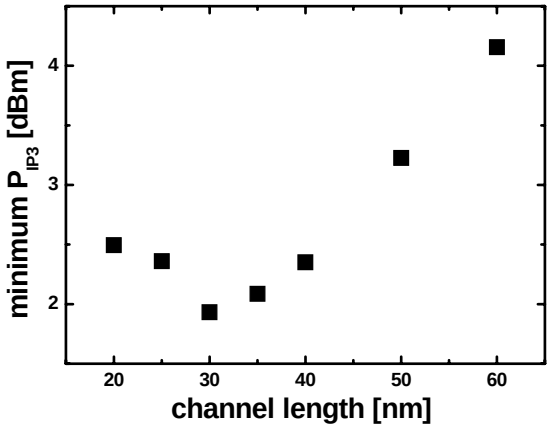

Fig. 3. Linearity performance of Double Gate MOSFET as a function of gate length.

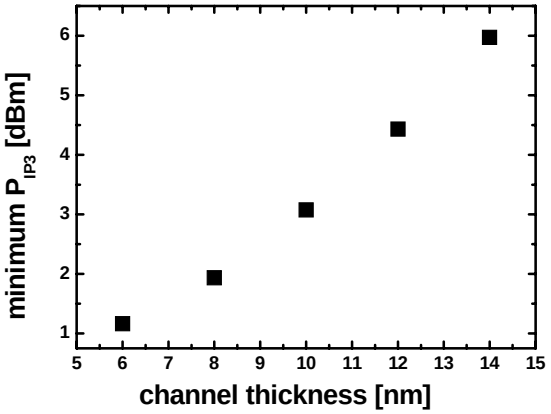

Fig. 4. Linearity performance of Double Gate MOSFET as a function of body thickness

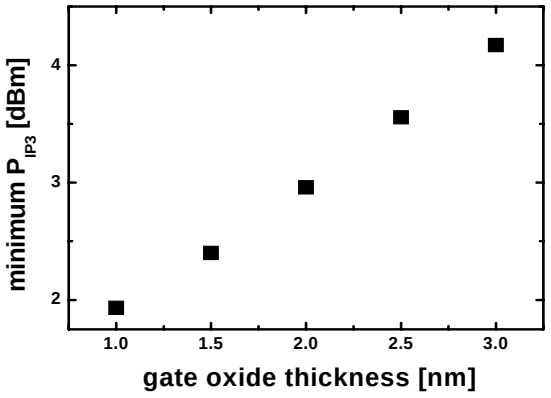

Fig. 5. Linearity performance of Double Gate MOSFET as a function of gate oxide thickness

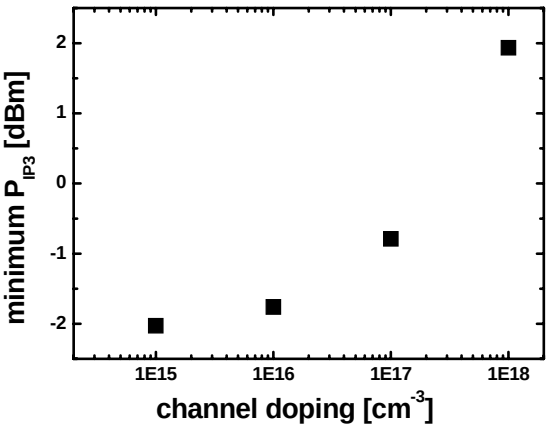

Fig. 6. Linearity performance of Double Gate MOSFET as a function of chaanel doping.

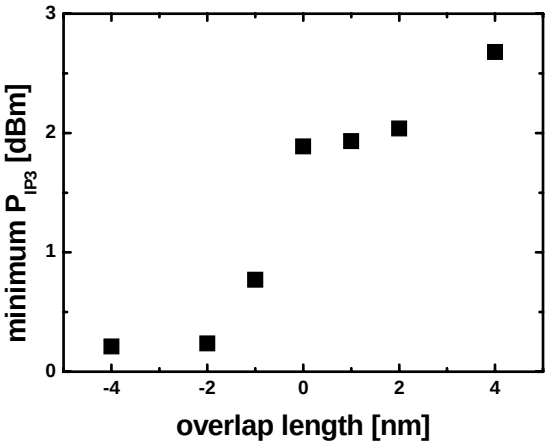

Fig. 7. Linearity performance of Double Gate MOSFET as a function of overlap length

IV. Conclusion

We have investigated using 2-D device simulations. RF linearity performance of DG MOSFETs as a function of device parameters such as silicon body thickness, gate length, oxide thickness, channel doping and overlap length. We observed that the linearity performance of DG MOSFETs decreases gradually as the gate length and gate oxide thickness is reduced. Too thin silicon body causes a bad performance of linearity. Linearity performance slightly increases with channel doping N_A. More overlapped structure between gate and Source/Drain region extends has a good linearity performance compared with non-overlap structure.

Acknowledgement

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Reference

[1] J. G. Fossum, et al., vol. 45, pp. 808-811, 2002

[2] Y-K Choi, et al., IEDM Tech.Dig., pp.421-424, 2001

[3] R. Chau et al., SSDM, pp. 68-69 , 2002,

[4] B Razavi RF Microelectronics, Prentice-Hall, 1998

[5] S Kang, et al., TED, 2003, vol. 3, no.8, pp. 972-977

[6] ATHENA & ATLAS User's Manual, Silvaco Int, 2000.

[7] W Ma, et al., EDMO, pp255-260, 2003.

[8] Savas Kaya, et al., EDL, vol.25, No. 5, pp. 308-310, 2004

[9] Burenkov, et al., ESSDERC pp. 135 – 138, 2003