

# Low Frequency Noise Characteristics of the 180nm MOSFETs

Youngchang Yoon\*, Hocheol Lee, In Man Kang, and Hyungcheol Shin

School of Electrical Engineering

Seoul National University

E-mail : \*y2chang@smdl.snu.ac.kr

## Abstract

**Performing accurate and repeatable low frequency noise measurement is critical for modeling and simulation of flicker noise. Through the accurate and repeatable on-wafer measurement, low frequency noise characteristics of the 0.18  $\mu\text{m}$  n-MOSFETs are discussed. And on-wafer flicker noise measurement system is presented. The on-wafer measurement system consists of cascade probe station, low noise current amplifier (SR570), and dynamic signal analyzer (HP35670A).**

## I . INTRODUCTION

CMOS transistors are often required as the core parts in analog circuit and applications owing to low voltage, density, and power consumption. Despite of the advantage of CMOS technology, there is a major drawback for analog applications. Low frequency noise is a performance limiting factor in many of today's CMOS analog and RF circuit. As the feature size of CMOS is scaled down to achieve higher speed and greater packing density, it has been reported that the low frequency noise will increase [1]. This increased low frequency noise is detrimental to the phase noise performance of high frequency non-linear circuit such as mixers and oscillators. It also deteriorates the signal-to-noise ratio in analog circuit [2].

In this paper, overall low frequency noise characteristics of n-MOSFETs including gate area, drain bias, and gate bias dependence have been presented and

on-wafer flicker noise measurement system is also presented. The on-wafer measurement system consists of cascade probe station, low noise current amplifier (SR570), and dynamic signal analyzer (HP35670A). The use of RF probes and Cascade station with the shielding box has rendered the need for shielding room unnecessary.

Larger gate area devices show much less relative sample-to-sample variance than small devices. In the case of small gate area, the noise power spectrum density shows many differently shaped spectra [3].

There is a growing consensus in the literature about the explanation of low frequency noise in n-MOSFETs in terms of carrier number fluctuations. Low frequency noise of the n-MOSFETs caused by carrier number fluctuation is inversely proportional to the number of carriers in the channel. So with increasing gate bias, more carriers exist in the channel. As a result, the level of relative spectral density of drain current fluctuations is decreased as increasing gate bias. Due to the same reason, the level of relative spectral density of drain current fluctuations is increased as increasing drain bias up to pinch-off point.

## II . Measurement System Description

The use of a LNA for low frequency noise measurement is critical. Fig.1 shows the measurement system.

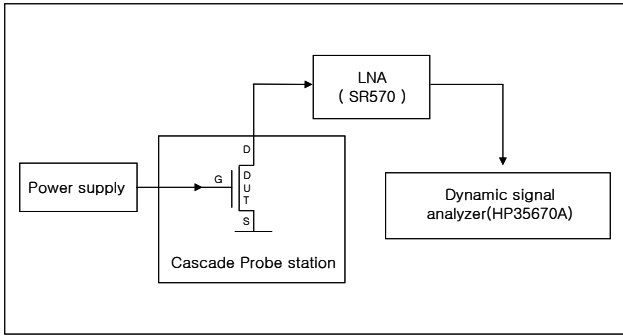


Fig. 1 Measurement system diagram

The SR570 is battery powered for low intrinsic noise. The output port of the MOSFETs is connected to the input of the LNA. There, it is biased to the desired voltage, and the drain current is taken up by the LNA. The gain of the LNA can be set over a wide range but there are the differences with intrinsic noise floor according to the gain. This fact should be considered while changing the value of the gain.

### III. MEASUREMENT RESULTS

The low frequency noise of the n-MOSFETs can be explained mainly by the carrier number fluctuations which are described by oxide charge tunnel trapping and de-trapping processes. The oxide trap cannot exist with complete uniformity in terms of both physical and energy aspects. As a result, it is obvious that there are more variations with oxide trap distribution in the case of smaller gate area devices. As the gate area becomes larger, the distributions of the traps become similar with each other [3].

Fig. 2 shows the measurement results of the four kinds of devices with different gate area of  $0.36\mu\text{m}^2$ ,  $1.8\mu\text{m}^2$ ,  $14.4\mu\text{m}^2$  and  $57.6\mu\text{m}^2$  respectively. Eight devices of each area which are with the same layout, but located on different position on the same wafer, are measured. There are four groups of measurement result in Fig. 2. To confirm the variation visually, we use double y-axis graph. Right-side y axis is set for the  $0.36\mu\text{m}^2$  case to avoid overlap with the  $1.8\mu\text{m}^2$  case. All of the devices are biased with gate voltage of 0.6 V and drain voltage of

0.1 V.

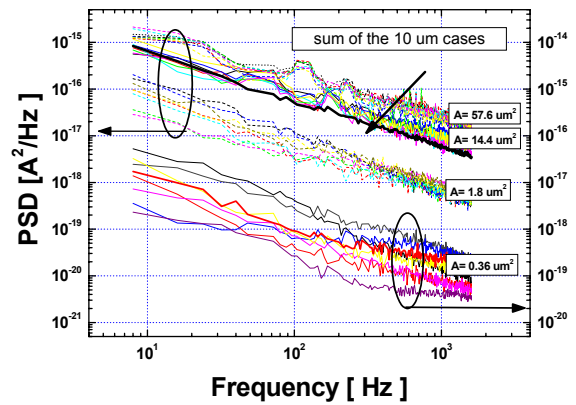


Fig. 2 Power spectrum density of the drain current in case of total area  $0.36\mu\text{m}^2$ ,  $1.8\mu\text{m}^2$ ,  $14.4\mu\text{m}^2$ , and  $57.6\mu\text{m}^2$

To confirm the variation visually, we use double y-axis graph. Right-side y axis is set for the  $0.36\mu\text{m}^2$  case to avoid overlap with the  $1.8\mu\text{m}^2$  case. The scale of both axes is the same. So comparison between each group can be performed directly on the graph. As expected, largest variation of the power spectrum density occurs in the case of the smallest devices.

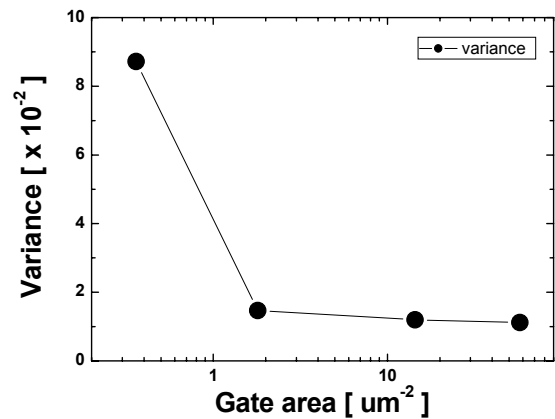


Fig. 3 Variation according to gate areas

Fig. 3 shows variation related with the result data above. The thick black line in Fig. 2 represents the sum of the eight cases of  $1.8\mu\text{m}^2$  devices. It can be verified that the summed data agree quite well with  $14.4\mu\text{m}^2$

devices. And in the case of  $0.36\mu\text{m}^2$  devices, the spectra show strong deviation from the  $1/f$  shape. Some of the cases even show random telegraph signal (RTS).

When considering number fluctuation, as the number of the carrier in the channel increases, the relative noise caused by trapping and de-trapping will be decreased. So the level of relative spectral density of the drain current fluctuation is decreased while increasing gate bias. [4].

There are measurement results of the  $3.6\mu\text{m}^2$  device in Fig. 4. When measuring the drain current noise spectra, gate bias is swept from 0.2 V to 1.2 V with fixed drain voltage, 0.1 V. The value of spectra is picked up at the frequency of 1 KHz. The decreasing relative noise dependency on the gate bias can be confirmed from Fig. 4. In Fig. 5 the  $3.6\mu\text{m}^2$  device is measured to verify the relative noise dependency on the drain bias. In this case, drain bias is swept from 0.1 V to 0.9 V with fixed gate voltage, 0.9 V.

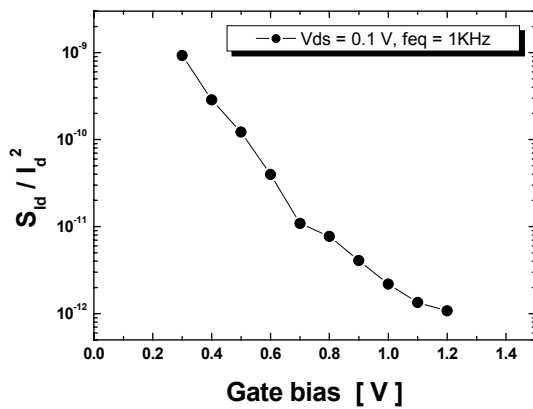


Fig. 4 Relative spectral density of drain current fluctuations according to the gate bias.

As increasing drain bias, the device is changed from the linear region to saturation region. In opposition to gate bias case, with larger drain bias, less carrier remains in the channel. And after pinch off point, the number of the carrier in the channel will be almost fixed. Fig. 5 shows that before pinch-off point, the relative noise is increased due to decreasing the number of carriers and after pinch-off the noise level is almost constant.

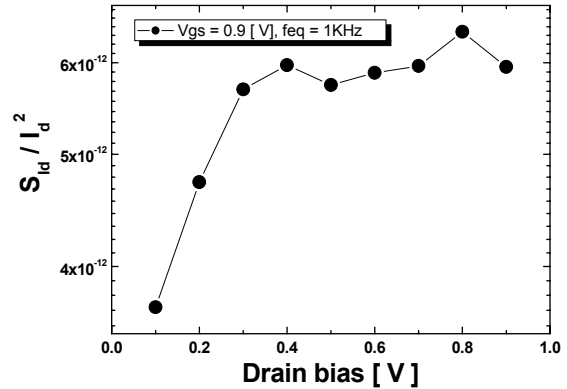


Fig. 5 Relative spectral density of drain current fluctuations according to the gate bias.

#### IV. CONCLUSION

On-wafer low frequency noise measurement system is presented. And through on-wafer measurement result, low frequency noise characteristics of the n-MOSFETs are discussed. In terms of gate area, it is verified that there are more variations with noise spectra in the case of smaller gate area devices. The noise dependency on bias condition is also presented.

#### ACKNOWLEDGMENTS

This work was supported by Samsung Electronics Co., Ltd., and ITRC.

#### REFERENCES

- [1] Tsai, M. H., and Ma, T. P., "The impact of device scaling on the current fluctuations in MOSFETs", IEEE Trans. Electron Devices, vol.41, no.11, pp.2061-2068, 1994
- [2] Hajimiri, A., and Lee, T. H., "A general theory of phase noise in electrical oscillators", IEEE Jour.

Solid-State Circ., vol.33, no.2, pp.179-194, 1998

- [3] A. J. Scholten, L. F. Tiemeijer, R. v. Langeveld, R. J. Havens, V. C. Venezia, "Noise Modeling for RF CMOS Circuit Simulation", IEEE Trans. Electron Devices, vol.50, no.3, pp.618-632, 2003
- [4] G. Reimbold, "Modified 1/f Trapping Noise Theory and Experiments in MOS Transistors Biased from Weak to Strong Inversion-Influence of Interface States", IEEE Trans. Electron Devices, vol.31, no.9, pp.1190-1198, 1984