스위칭 엑티비티를 최소화한 저전력 DCT 아키텍쳐 구현

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Low-Power DCT Architecture by Minimizing Switching Activity

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요 약

Low-power design is one of the most important challenges encountered in maximizing battery life in portable devices as well as saving energy during system operation. In this paper we propose a low-power DCT (Discrete Cosine Transform) architecture using a modified Computation Sharing Multiplication (CSHM). The overall rate of power consume is reduced during DCT: the proposed architecture does not perform arithmetic operations on unnecessary bits during the Computation Sharing Multiplication calculations. Experimental results show that it is possible to reduce power dissipation up to about 7~8% without compromising the final DCT results. The proposed low-power DCT architecture can be applied to consumer electronics as well as portable multimedia systems requiring high throughput and low-power.

1. Introduction

The DCT [5] was developed by Ahmed, Natarajan, and Rao in 1974. It has become one of the most widely used transform techniques used in digital signal processing. In the recent year, DCT applications have been extended to portable multimedia devices such as PDA and IMT-2000 cellular phones. For those applications, low-power design [6] is one of the key issues to consider in order to prolong the battery life of the portable devices. Therefore, many designers consider low-power as well as high speed when designing those portable devices.

In a CMOS circuit, power consumption can be reduced by using smaller switching activity in the circuit as expressed in the following equation (1).

$$P_{switching} = aCV^2_{dd} f_{clk} \quad (1)$$

Where 'a' is the switching activity parameter, 'C' is the loading capacitor, V_{dd} is the supply voltage, and F_{clk} is the operating frequency. The symbol 'aC' can also be viewed as effective switching activities when measured at the capacitor node, during charging and discharging. The only parameter which can be reduced at an algorithmic level is the switching activity. Therefore, minimizing the switching activity in the algorithmic level during the multiplication process should be considered first, before the complex and expensive process of implementing a multiplier is attempted [10].

The DCT is one of the computationally intensive transforms which require many multiplications and additions. Many DCT algorithms were proposed in order to achieve low-power DCT operations. The current architecture using multipliers has less regular VLSI architecture due to complex routing and requires large silicon area. On the other hand, the DCT architecture based on the Distributed Arithmetic (DA) algorithm [7] leads to regularity as well as modularity suitable for VLSI implementation. The DA algorithm has the advantage that no multiplication operations are necessary, since it used look-up tables for multiplications. However, as the number of inputs and internal precision increase, DA needs a large size of ROM, thus greatly increasing the hardware complexity. Moreover, since DA is a bit serial operation, it needs unfolding [8] or pipelining [9] for high performance.

In this paper, we propose a low-power DCT architecture using modified Computation Sharing Multiplication (CSHM), based on the DCT algorithm. The proposed architecture skips unnecessary arithmetic operations which occur during CSHM

computation without compromising the final DCT results. We verify this low-power algorithm using C language, model its algorithm in the RTL level using Veilog, synthesize the HDL model using 0.25 ㎛ technology, and perform P&R(placement and routing) to achieve the final layout. After extracting parasitics and delay information from the layout, we estimate the power dissipation of the proposed DCT. Experimental results show that the proposed architecture consumes at maximum power consumption operational levels, 7~8% less power than the conventional CSHM-based DCT architecture.

This paper is organized as follows: the CSHM-based DCT algorithm is described in Section 2. In Section 3, we propose the low-power DCT architecture. The experimental results are shown in Section 4. Finally concluding remarks are described in Section 5.

2. Computation Sharing Multiplication Algorithm

Vector Scaling operation [1,2] refers to the multiplication of vectors by scalars.

In this paper, we propose a modified DCT architecture based on a computation sharing multiplier, which targets the reduction of redundant computation used in the multiplication of vectors by scalars.

In the vector scaling operation if we carefully select a set of small bit sequences, the same multiplication result can be obtained by utilizing add and shift operations only. For instance, a simple vector scaling operation 1C•[X0, X1], X0=01100111, X1=10001011, can be deconstructed as X0•C= 2^5•(0011)•C+(0111)•C, X1•C= 2^7•(0001)•C + (1011)•C If C, (0011)•C, (0111)•C and (1011)•C are available, the entire multiplication process is reduced to a few add and shift operations. [1] In Figure 1, the PRECOMPUTER performs the multiplication of 4 bits of input, calculated with coefficients. The 8bits of input signals for the eight PRECOMPUTERS represent small bit sequences

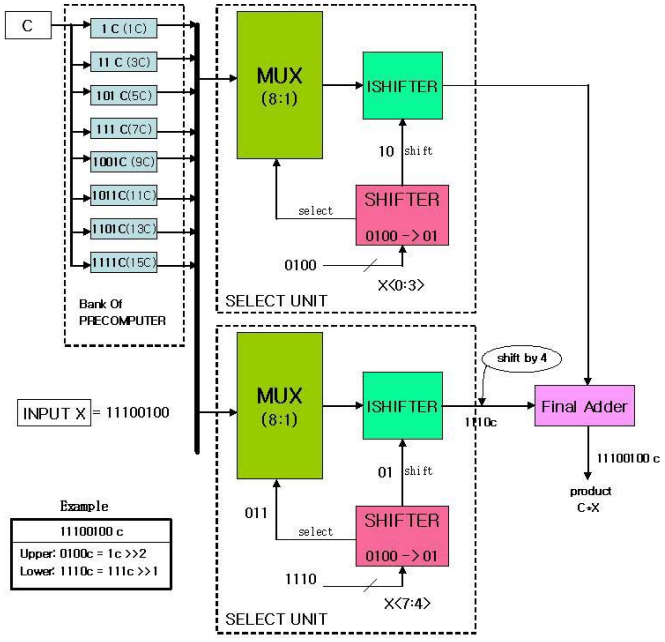


Figure1: Computation sharing multiplier structure

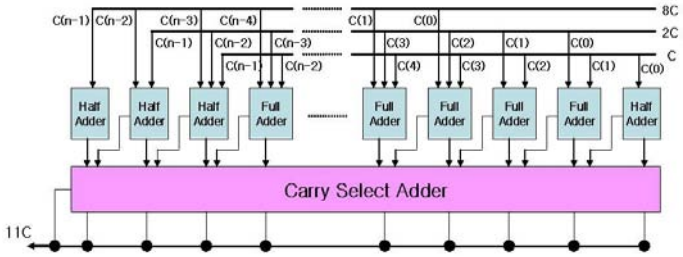


Figure 2: Precomputer (11c) architecture. (a) 11c(1011c)=8c(1000c)+2c(10)c+c (<<<3) (< 1)

3. The proposed low-power DCT architecture

For low-power DCT, we propose a DCT architecture which reduces the switching activity in the Bank of PRECOMPUTERS and SELECT_UNITS without experiencing a loss in precision.

If the image data stored in an 8x8 block has similar values, the probability that the same values enter as input to the PRECOMPUTERS and SELECT_UNITS will be high. This 8-bit input is separated into two groups, and then each group is compared by a comparator. The first group repesents the first four MSBs and the second group contains the next four LSBs. Such input data has no effect on the final results even if the calculation, repeating first four MSBs or four LSBs are skipped. For instance, the first four for 8 bit input data MSBs 01110010 and 01110011 are the same. Therefore, only four LSBs needs multiplication and the four MSBs can be skipped. We can simply demonstrate this expression as follows (2):

$$X_i = 01110010$$
$$X_{i+1} = 01110011 \qquad (2)$$

In case (2), if the first four MSBs in X_{i+1} are the same with the first four MSBs of X_i, then experimental results indicate that repetition can be ignored during multiplication. The proposed repetition skipping method utilized during PRECOMPUTERS and SELECT UNIT arithmetic operations has been simulated using real-life images as shown in Table 1. Figure 3 shows the images used in this experiment. The Miss America image, which has many low frequency components, demonstrates larger skipping ratio necessary for repetition than that of the Flower Garden image, which has many high frequency components: since low frequency regions in an image tend to have similar pixel values, the input data of the PRECOMPUTERS function in low frequency regions have smaller values approaching zero. The Lena image, which has both high and low frequency components presents a medium skipping ratio.

We analyzed the input skipping ratios of the proposed modified CSHM scheme used for DSP applications. We obtained operational results for the DCT. The QCIF images (Lena, Flower Garden, Miss America) were used in analysis, as shown in Figure 4. As presented in Table 1, 8x 8 DCTs of each image require 84480, 358848 and 65536 multiplications in these experiments. The entire multiplication process is reduced to a large number of add and shift operations in the modified CSHM.

Therefore, the experimental results indicated that a DCT, using modified Computation Sharing multiplication, can reduce total power consumption.

Table 1. Skipping ratio of the proposed algorithm

Images	Miss America	Lena	Flower Garden
4 MSB bits skip (Ratio)	70629 (83.604 %)	166843 (63.646 %)	29746 (46.805 %)
4 LSB bits skip (Ratio)	38298 (45.334 %)	24341 (9.285 %)	7310 (11.154 %)
Total calculation	84480	262144	65536

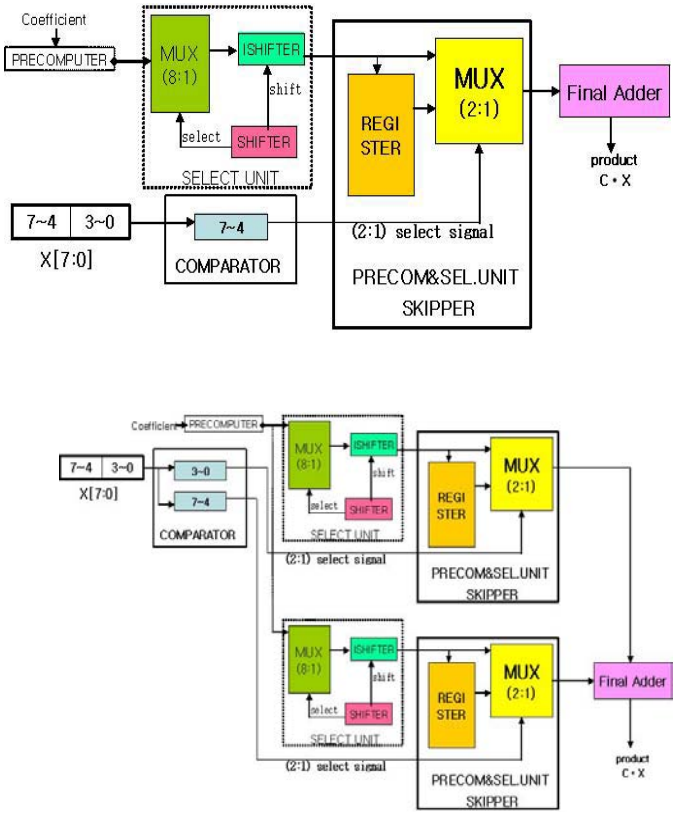
(a) Lena

(b) Flower Garden

(C) Miss America

Figure 3. Test images.

The proposed architecture is a modified CSHM as shown in Figure 4. Unnecessary repetition can be reduces by adding a comparator, and a multiplexer. If the input value of DCT is 8 bits ranging from 00000000 to 11111111, the first four MSBs or next four LSBs are the same before input. Therefore, we can check unnecessary repetition conditions by adding a simple comparator as shown in Figure 5. This comparator is designed to have minimal switching activity by using only the first four MSBs or LSBs.



(b) four MSB and four LSB skip

Figure 4. The proposed DCT Architecture

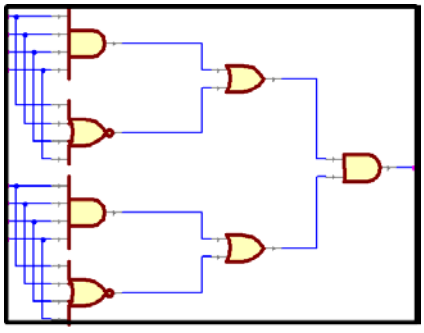


Figure 5. comparator

4. Implementation and experimental results

We estimated total power dissipation using the layout result of the proposed DCT architecture. Figure 6 displays implementation and experiment's flow chart:

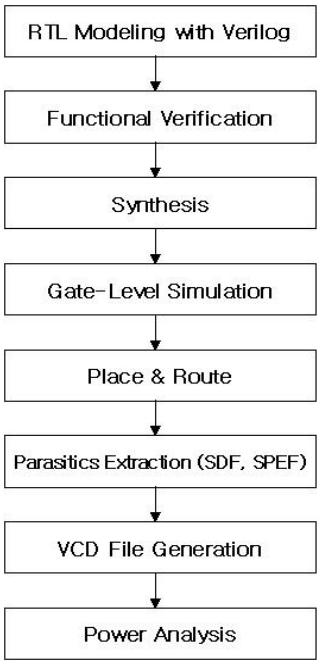


Figure 6. Experiment flowchart

We designed and estimated both conventional DCT architecture as well as the proposed architecture. After modeling the two architectures using Verilog, the functions of both architectures were verified, and netlists were extracted. After P&R using a Apollo II tool, SDF(standard Delay Format) and SPEF(Standard Parasitic Extraction Format) files were extracted. Then, VCD (Value Change Dump) files were generated by using netlists, SDFs, and Verilog cell libraries using a VCS 7.0 tool. Using VCD, SPEF, netlists, and libraries, which include the power information, we estimated and compared power dissipation levels for several images using a Synopsys' PrimePower tool. Furthermore, the delays of both architectures were measured. Finally, we used Hynix 0.25 ㎛ CMOS libraries in this experiment.

Table 2. Power analysis (unit: ㎽)

	Miss America	Lena	Flower Garden
4 MSBs skip (Ratio)	15.01 (92.20 %)	15.09 (93.32 %)	15.67 (93.51 %)
4 MSBs and 4 LSBs skip (Ratio)	14.93 (91.71 %)	15.01 (92.84 %)	15.64 (93.32 %)
CSHM	16.28	16.17	16.76

Since the Miss America image has many low frequency components (many similar pixel values located in sub-images), the power reduction ratio is higher (about 8%) than the other images.

Both four MSBs and four LSBs also demonstrate a lager skipping ratio. Since the Flower Garden image has a relatively higher number of frequency components, the power reduction ratio is smaller. For most images, we can observe that the proposed architecture can reduce the power dissipation. This high power reduction ratio is especially, evident in images that have a simple background.

5. Conclusion

In this paper, we proposed a novel low-power DCT architecture using the modified CSHM. In order to reduce overall power dissipation, we can check the unnecessary repetition conditions by adding a simple comparator. The proposed architecture reduced the total number of repetition computations performed on the input data four MSBs or four LSBs for the CSHM, because the number of repetition operations, in CSHM based DCT computation was reduced by utilizing the fact that most images have similar neighboring pixels. The power dissipation of the proposed DCT architecture can reduced up to 7~8% when compared with the conventional DCT architecture. Therefore, the proposed DCT architecture can be applied to portable multimedia devices as well as consumer electronics.

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