고분자 기판 상에 제작된 극저온 다결정 실리콘 박막 트랜지스터에 관한 연구

김영훈, 김원근, 문대규, 한정인
전자부품연구원 디스플레이연구센터

Fabrication of Ultra Low Temperature Polycrystalline Silicon Thin-Film Transistors on a Plastic Substrate

Yong-Hoon Kim, Won-Keun Kim, Dae-Gyu Moon, Jeong-In Han
Information Display Research Center, Korea Electronics Technology Institute

Abstract : This letter reports the fabrication of polycrystalline silicon thin-film transistors (poly-Si TFT) on flexible plastic substrates using amorphous silicon (a-Si) precursor films by sputter deposition. The a-Si films were deposited with mixture gas of argon and helium to minimize the argon incorporation into the film. The precursor films were then laser crystallized using XeCl excimer laser irradiation and a four-mask-processed poly-Si TFTs were fabricated with fully self-aligned top gate structure.

Key Words : poly-Si TFT, XeCl excimer laser, plastic substrate, sputter

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are currently used in active-matrix flat panel displays (FPDs) as pixel switching devices and also as peripheral drive circuit elements. The monolithical integration of drive circuits into the panels reduces the external interconnection to the panels and improves the form/factor of the displays.

In general, the poly-Si TFTs are fabricated on glass or quartz substrates using amorphous silicon (a-Si) precursor films formed by plasma-enhanced chemical vapor deposition (PECVD). However, PECVD deposited films contains considerable amount of hydrogen atoms (10~20 at%) which causes ablation of Si films during the laser annealing process. To eliminate the film ablation problem, dehydrogenation process is carried out before the laser annealing to remove the excess hydrogen atoms. However, most of the polymer substrates have maximum temperature limits under 300°C, thus an alternative laser dehydrogenation is frequently used in the case of using polymer substrates [1]. In contrast to PECVD deposition, sputtered a-Si films can have very low concentration of impurities (<1~2 at%), suggesting that it is a very attractive method for realizing high performance active-matrix displays using polymer substrates.

2. Experimental Details

Here, the plastic substrate was pre-annealed at 180°C (for PES; polyethersulfone) or at 250°C (for PAR; polyarylate) in a vacuum oven before the fabrication. After the pre-annealing, substrate was coated with 600-nm-thick SiO_2 buffer layers on both sides. Then a-Si precursor film was deposited on thebuffer layer using a sputtering system with argon/helium mixture gas at 110°C. The substrate was then laminated onto a glass substrate using a thin adhesive film and irradiated by XeCl excimer laser (λ=308 nm) having a flat top beam profile. The pulse duration and the beam size of the laser were 35 ns and 45 x 0.2 mm^2, respectively. After defining AlNd gate electrode (sputter, 200-nm-thick) and gate insulator (PECVD, 200-nm-thick), ion shower process was carried out to dope the Si layer and activated with XeCl laser. Then 400-nm-thick interlayer dielectric was deposited and contact hole was defined. Finally, 300-nm-thick AlNd source and drain electrode was deposited and patterned.

3. *Results and Discussion*

One of the disadvantages of using polymer substrates instead of glass is the large dimension changes during thermal cycling procedure. Upon heating a polymer material, structural changes take place which can be divided into a reversible part controlled by coefficient of expansion (CTE) and an irreversible part given by coefficient of shrinkage [2]. Although the CTE mismatch between the polymer and inorganic films induces considerable stress in the film-substrate system, the shrinkage of polymer may also give a critical limitation to TFT fabrication since it is an irreversible process. In order to reduce the effect of irreversible shrinkage during TFT fabrication, the substrates must be annealed before the process starts as mentioned above. The shrinkage rates were noticeably decreased with annealing time more than 60 hours. For PAR substrates, the rates decreased from 30 ~ 50 ppm/K to less than 2 ppm/K and for PES, the rates decreased from 180 ~ 200 ppm/K to 2 ppm/K, which are in the acceptable range for TFT

fabrication.

After deposition of double-sided SiO_2 buffer layers, a-Si film was coated by sputtering in argon/helium mixture atmosphere. The argon impurity concentration in the a-Si film was controlled by adjusting the argon/helium mixture ratio and working pressure. The Argon concentrations in Si films were measured by Rutherford backscattering spectrometry (RBS). As a result, there was a clear relationship between the argon concentration and the argon/helium ratio. Particularly, with argon/helium ratio of 2:20, the argon concentration in the film was determined as 1.6 at%, whereas with argon/helium ratio of 2:5, the argon concentration was 6.0 at%.

The a-Si film was laser annealed at room temperature in vacuum atmosphere. During the laser annealing process, ablation of Si film was observed in samples with buffer layer thickness of 400 nm, whereas no ablation was occurred when the buffer layer thickness was increased to 600 nm. This suggest that there exists a critical buffer layer thickness using a substrate having low thermal stability since the substrate experiences an extremely high temperature increase during the short period of laser annealing process. Figure 1 shows the transmission electron microscopy (TEM) images of poly-Si films irradiated with various energy densities. The grain size increased from 10 nm to 400 nm when the laser energy density was changed from 200 mJ/cm^2 to 289 mJ/cm^2.

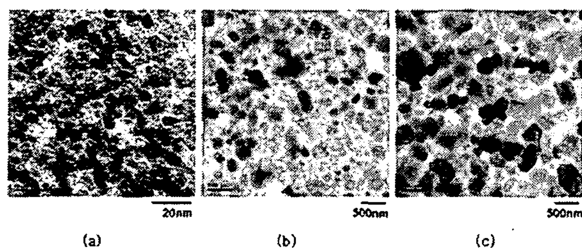

Fig. 1. TEM images of laser annealed poly-Si films irradiated by various laser energy densities

Ion implantation or ion shower doping is widely used for the low-temperature poly-Si TFT fabrication [3]. Although the ion shower doping without mass separation has problems of reproducibility and controllability in low-dose doping, the ion implantation also has a problem in throughput for high-dose doping [3]. In this research, ion shower doping method was used to dope the Si films. The doping temperature and acceleration voltage were room temperature and 10 kV, respectively. The sheet resistances of 470□/sq. for boron doping and 1200□/sq. for phosphorus doping were successfully obtained on polymer substrates and these values are low enough for the source and drain formation in poly-Si TFTs.

The transfer characteristics of fabricated nMOS and pMOS TFTs are displayed in Fig. 2. The nMOS TFT showed field-effect mobility of 25 cm^2/V·s, on/off ratio of 10^5 and threshold voltage of 5V, while the pMOS TFT showed field-effect mobility of 32 cm^2/V·s, on/off ratio of 10^5 and threshold voltage of -2V. The leakage currents in the devices were 30 pA and 1 pA for nMOS and pMOS TFTs, respectively, which are relatively low for devices without lightly doped drain architecture.

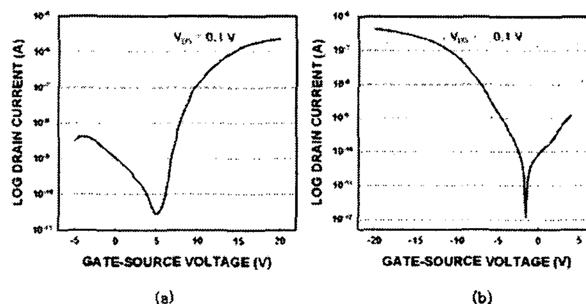

Fig. 2. Transfer characteristics of fabricated (a) nMOS and (b) pMOS poly-Si TFTs on polymer substrates.

4. Conclusions

In this report, the fabrication of poly-Si TFTs on flexible polymer substrates using sputtered deposited a-Si films was discussed. It was found that the argon impurity concentration was dependent on the argon/helium mixture ratio. The precursor films were then laser crystallized using XeCl excimer laser irradiation and a four-mask-processed poly-Si TFTs were fabricated with fully self-aligned top gate structure.

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