$\mathbf{Au} \ \mathbf{Q} \ \mathbf{Au/SiO_2} \ \mathsf{L}\mathbf{V}$ 나노입자를 이용한 나노부유게이트메모리 단일소자의 전기적특성

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Electrical Properties of Nano Floating Gate Memory for Using Au and Au/SiO2 Nanoparticles

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Abstract: Au and Au/SiO₂ nanoparticles(NPs) were synthesized by the colloidal method. The formation of Au and Au/SiO₂ NPs was confirmed using high resolution transmission electron microscopy (HRTEM). Synthesized solutions were deposited on Si wafer. The electrical properties of structures were measured using a semiconductor analyzer and a LCR meter. Capacitance versus voltage hysterisis curves showed the charge storage effect by Au and Au/SiO₂ NPs.

Key Words: Au, Au/SiO2, Nano floating gate memory

1. Introduction

Nanoparticles(NPs) of metalsand semiconductors are currently the focus of remarkable research. Among them, nonvolatile memory devices based on localized charge trap sites such as metal nanoparticles and silicon oxide nitride oxide silicon(SONOS) have much attraction due to their lower power consumption and smaller scalability compared to the conventional flash memory devices.[1]

However, in order to obtain flash memory devices for the more stability and reliability, we need to develop technologies for both a fast write/erase speed and a longer retention time. For this purpose, metal nanoparticles have been recommended as the charge storage. By controlling the work function of metal nanoparticles, they provide a high barrier layer for longer retention time and a thin barrier layer for lower write/erase voltages.[2]

Nonvolatile memory is one of the fancy metal oxide silicon(MOS) device. The top electrode forms the control gate, below which a floating gate (metal nanoparticles) is coupled to the control gate and the underlying tunneling oxide. In this paper, we have investigated the formation and electrical properties of Au and Au/SiO₂ nanoparticles as the charge storage.

2. Experiment

2.1 Synthesis

Solution of ~6nm Au NPs in toluene was prepared as a following description.[3] Au/SiO₂ NPs in water was prepared as using solution of Au NPs.[4] For high resolution transmission electron microscopy(HRTEM) studies, we confirmed the synthesized Au and Au/SiO₂ NPs and resulting HRTEM micrographs are shown

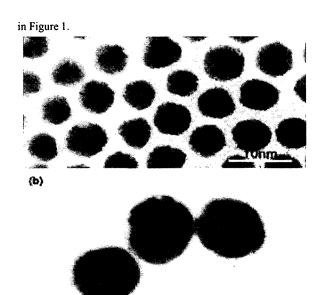


Fig 1. High resolution transmission electron micrographs of Au (a) and Au/SiO₂ (b) NPs

10nm

2.2 Fabrication

silicon(p-type, (100) orientation) wafers with a 6.3nm thermally grown oxide layer were used as the substrates. Prepared solutions were deposited on silicon substrates by spin-coating at 1500~6000rpm. After dried off the solvent, Al₂O₃ was deposited on the substrates by atomic layer deposition (ALD) for control gate oxide. A deposition thickness of control gate oxide was 60nm. Following control gate oxide deposition, Al control gate material was thermally evaporated in a vacuum chamber onto the films through a metal shadow mask. Figure 2 shows the various structures that were investigated in this work: (a) Al / Al₂O₃ / SiO₂

/ p-Si, (b) Al / Al₂O₃ / Au NPs / SiO₂ / p-Si, and (c) Al / Al₂O₃/ SiO₂ capped Au NPs / SiO₂ / p-Si

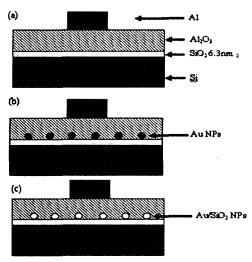


Fig 2. Schematic diagrams of different structures.

3. Result and Discussion

The electrical characteristics of above structures were measured using a semiconductor analyzer and a precision LCR meter. Figure 3 shows the normalized capacitance versus voltage(C-V) curves, at measured 1MHz and a sweep rate of 0.2V/s. The C-V curve for the reference Al₂O₃/SiO₂/Si sample reveals the usual characteristics and shows a negligible hysteresis. But, samples with containing Au NPs or Au/SiO₂ NPs show the larger width of hysteresis curves. This result may be caused by the charge trapping sites buried in an Al₂O₃ control oxide layer.[5, 6] The data in Figure 3 reveal that the flat band voltages of Au NPs solution coated film and Au/SiO2 solution coated film are approximately -2V and -1V, shifted by 0.5~1V when compared to a film which not coated. This suggests that the anion ion like Na⁺ has some positive charge at the interfacial states or within control oxide layer, i.e.. The more large flat-band voltage(VFB) shift is obtained as shown figure 4. After biasing voltage stress (±10V for 0.1sec), samples with Au and Au/SiO2 NPs shows VFB shift of

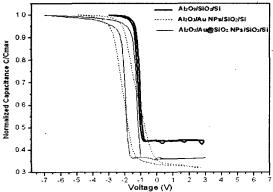


Fig 3. C-V characteristics for the difference device configurations investigated. (Figure 2).

2.5V and 3.5V. When the negative bias applied to the control gate, electrons may are ejected from Au and Au/SiO₂ NPs. The opposite condition occurs in the inversion region, and electrons may are injected from Si wafer.

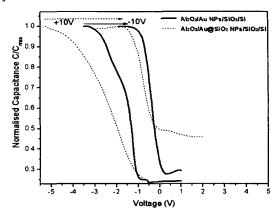


Fig 4. C-V curves after biasing voltage stress to samples.

4. Conclusion

Au and Au/SiO₂ nanoparticles (NPs) were synthesized by the colloidal method. The formation of NPs was confirmed using HRTEM. Synthesized solutions were deposited on p-type Si wafers with a 6.3nm thermally grown oxide. And alumina layer (control oxide) was deposited on top of the nanoparticles to form a MOS by atomic layer deposition. Measurements of capacitance versus voltage (C-V) hysteresis curves showed the charge storage effect by Au and Au/SiO₂ NPs that were into alumina layer.

Acknowledgements

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