Current Uniformity Enhancement for AMOLED Data Driver IC

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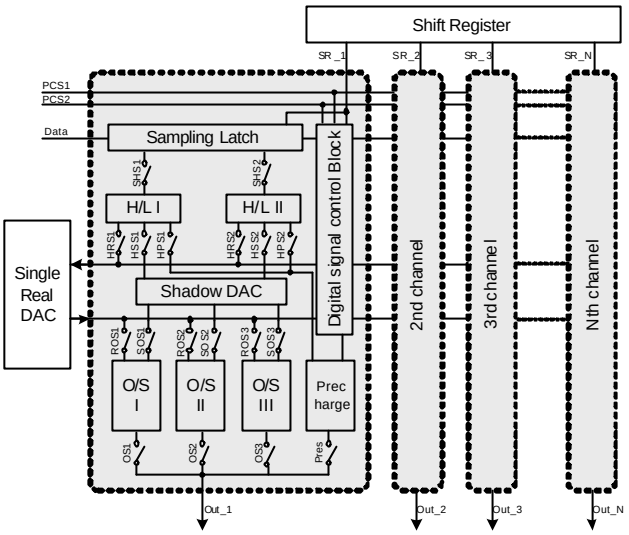
Abstract
A novel current-type data driver for active matrix organic light emitting diode (AMOLED) is proposed for current uniformity enhancement among its output channels. New architecture is composed of shadow DACs that precharge output stages, a single-real DAC that correct the output level to a real target current level and output stages that operate in 3 states of sampling, correcting and driving. Simulation results show that the proposed driving method and circuits improve the current uniformity among output channels of a current-type driver IC.

1. Introduction
Even though OLEDs have attractive advantages as future FPDs such as wide viewing angle, fast response, low power consumption, and thin panel thickness [1], much more effort is required to be widely used because of obstacles coming from the current driven nature. An OLED data driver can be either voltage-type or current-type depending on the pixel structure. Research activities on the current-type data driver are vigorously progressing because current-type pixel circuits can compensate panel imperfections such as Vth and mobility non-uniformities of TFTs and IR drop of the supply voltage. In a current-type data driver, however, the uniformity of its output currents especially between neighboring outputs and managing low-level current are of critical importance. Several current-type data drivers have been proposed for overcoming these issues [2],[3],[4]. However, for low-gray-level current, the current-type data drivers still suffer from poor uniformity of outputs due to either different parasitic RC of signal lines wiring a current DAC and output stages or transistor mismatch or both. To simultaneously satisfy two unresolved problems, uniformity and low-gray-level current, Current Sampling and Correcting method, CSC, has been proposed.



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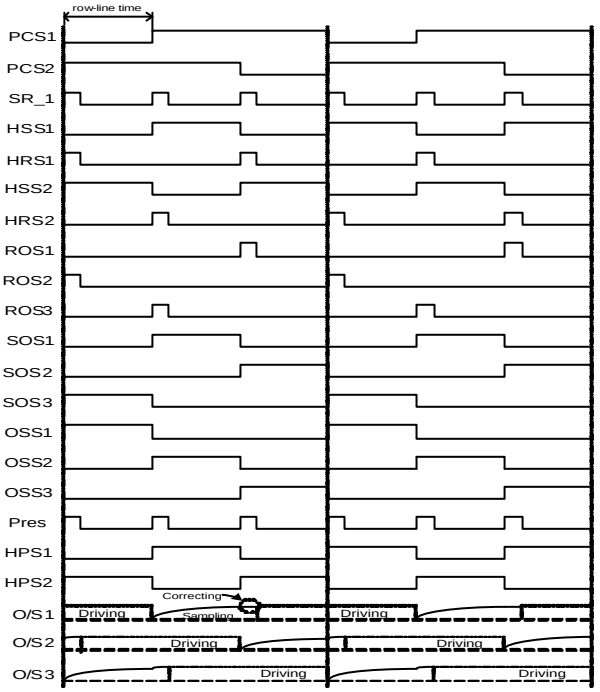


(b)

Figure 1. (a) Block diagram of proposed data driver, (b) timing-chart of proposed data driver

2. Proposed Driving Method

Figure 1 (a) shows the block diagram of proposed current-type data driver, where one channel is illustrated in detail. The proposed current-type data driver has single current-type DAC and one channel includes sampling latch, two holding latches, shadow current-type DAC and three output stages. Unlike a conventional data driver two holding latches allow to utilize two row-line-time for data conversion and driving the panel. In the first data conversion time, data from one holding latch is transferred to shadow current-type DAC included in each channel and sampled by one output stage and in the second data conversion time, data is transferred to single-real DAC to correct the sampled current to the real target current level during point-time which is defined in Eq. 2. The single-real DAC is shared by all channels, so that all channels can have the same output current in spite of the non-uniform characteristics among channels.

$$\text{row-line time} = \frac{1}{\text{frame rate} \times \#\text{ of row lines}} \quad (1)$$

$$\text{point time} = \frac{1}{\text{frame rate} \times \#\text{ of row lines} \times \#\text{ of channel}} \quad (2)$$

Figure 1 (b) shows the operation of current sampling, correcting and driving of O/S1, O/S2, and O/S3 with the control signals. Data transferred from sampling latch to holding latch is maintained in holding latch for two row-line-time to decrease switching error influence on output stages. As shown in Figure 2, each output stage operates in three state, sampling, correcting and driving.

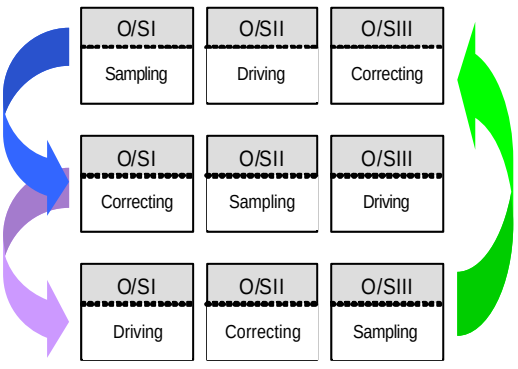
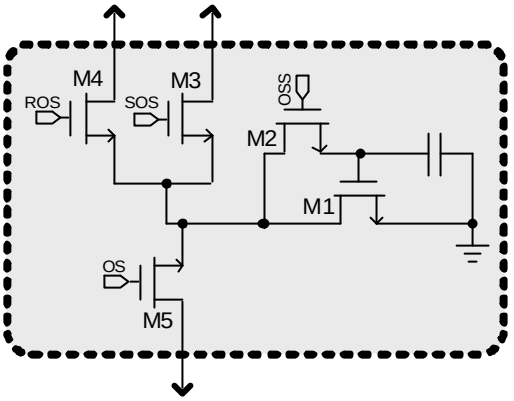


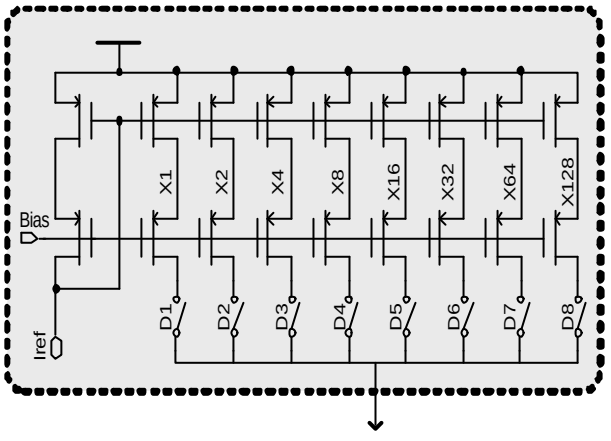
Figure 2. Block diagram for 3state operation of output stages

3. Circuit Configuration

Figure 3 (a) shows one output stage where switches connected to H/L and an output port are included. When either ROS or SOS switch is on, OSS is on, and OS is off. This state is either sampling or correcting depending on which switch is on between ROS and SOS. When OS switch is on, the output stage drives the panel. In Figure 3 (b) 8-bit current-type D/A converter is shown. Current sources are composed of P-type transistors that have weighted width with their multiplication factor, and switches are controlled by binary weighted data signals (D1~D8) [5].



(a)

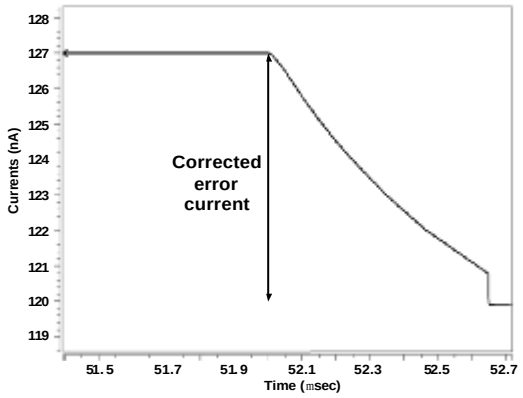


(b)

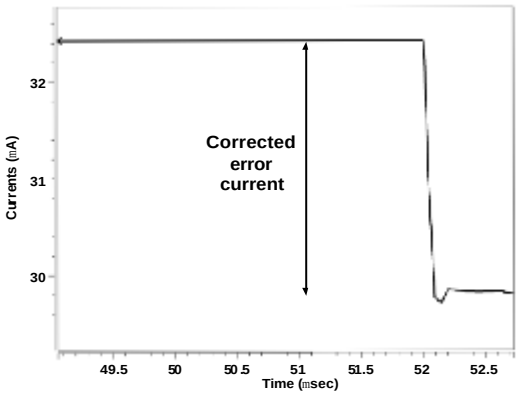
Figure 3. Schematic diagrams (a) output stage circuits, (b) current-type DAC circuits

4. Simulation

We confirmed CSC method for AMOLED application through HSPICE simulations [6]. To consider practical situation into our simulation, parasitic resistance and capacitance between DAC and output stages are extracted by RAPHAEL [7] and presented in Table 1 with other simulation conditions. Figure 4 (a) and (b) are the simulated current waveforms of the current-type data driver during the sampling and correcting period at output stages, and the simulation conditions are summarized in Table 2. Because we used binary weighted current-type DAC, the output current error in LSB caused by Vth variations is multiplied by its weighted code for the worst case. Figure 5 (a) and (b) shows the error percentage of output currents with Vth variations. It is found that as the gray-scale goes up, the error correction gets more remarkable with CSC.

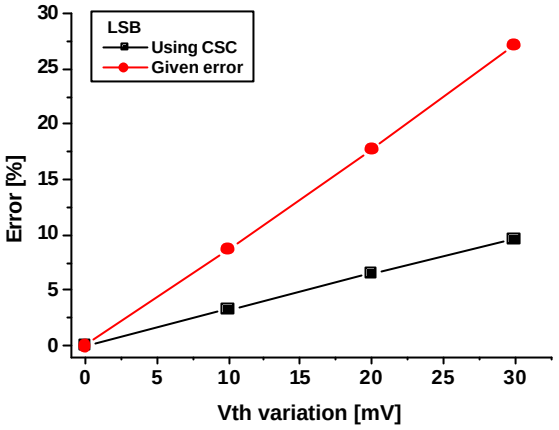


(a)

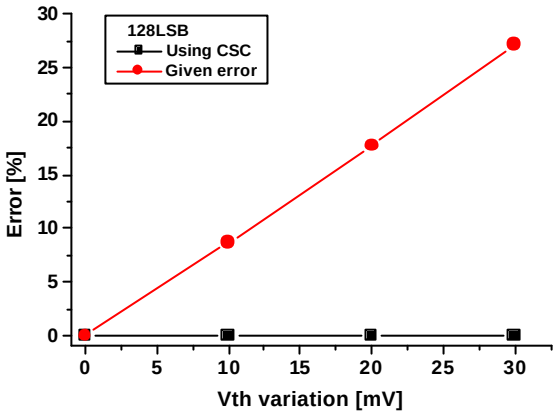


(b)

Figure 4. Simulated current waveforms (a) 1-LSB, (b) 255-LSB



(a)



(b)

Figure 5. Simulation results with Vth variations, (a) 1 LSB, (b) 128 LSB

Table1. panel specification and simulation conditions

Item	Specification
Format	240 x RGB x 320
Gray scale	256 gray
Frame rate	60 Hz
Number of output channel	240
Output current range	117nA~30μA
row-line time	52μsec
point time with 3(RGB) DAC	651nsec
Parasitic resistance of line	50Ω
Parasitic capacitance of line	5pF

Table 2. DAC output current fluctuation from assumed Vth variation

	Ideal	10mV Vth variation
1-LSB	117nA	127nA
255-LSB	29.835μA	32.425μA

5. Conclusion

We propose a novel configuration of a current-type data driver to attack the issue of the current uniformity especially for low-gray-level current. As found from the simulation results, CSC method can successfully overcome the non-uniformity due to either different parasitic RC of signal lines wiring a current DAC and output stages or transistor mismatch or both. Using shadow DACs and 3state operating output stages obtains the current uniformity among output stages by correcting with a single-real DAC. Therefore, CSC method is well suited to the current-type data driver IC for AMOLED application.

6. References

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