Hysteresis Behavior in Pentacene Organic Thin-film Transistors

Myeong-Seob So, Min Chul Suh, Jae-Bon Koo, Byoung-Deog Choi,
Dae-Chul Choi, Hun-Jung Lee, Yeon-Gon Mo, Ho-Kyoon Chung

Corporate R&D Center, Samsung SDI Co., LTD., 428-5 Gongse-Ri, Kiheung-Eup, Yongin-City, Kyungki-Do, 449-902, KOREA.
TEL : +82-31-288-4735, E-mail: mcsuh@samsung.com

Abstract

In this paper, we have identified the mechanism of C-V hysteresis behavior often observed in pentacene organic thin-film transistors (OTFTs). The capacitance-voltage (C-V) characteristics were measured for pentacene OTFTs fabricated on glass substrates with MoW as gate/source/drain electrode and TEOS SiO_2 as gate insulator. The measurements were made at room temperature and elevated temperatures. From the room temperature measurements, we found that the hysteresis behavior was caused by hole injection into the gate insulator from the pentacene semiconductor for large negative gate voltages, resulting in the negative flat-band voltage shift. However electron injection was observed only at elevated temperatures

1. Introduction

Organic thin-film transistors (OTFTs) are being extensively studied for a variety of applications. Since OTFTs can be processed at low temperatures compatible with plastic substrates, they are competitive candidates for TFT applications requiring large-area coverage, structural flexibility, and especially low cost. Such applications include radio-frequency identification (RFID) tags, digital paper displays, back planes for flexible active-matrix liquid crystal displays (AMLCDs) and organic light-emitting diodes (AMOLEDs).

The device performance of OTFTs has improved dramatically over the last decade. Groups at Pennsylvania State University, Philips Research, and Lucent Technologies have recently demonstrated integrated circuits [1-4] and active-matrix displays [5-8] based on OTFTs. The device performance of OTFTs has often been measured by the carrier field-effect mobility. There has been a continuous increase in mobilities recently due to the improvements in the processes such as thermal vacuum evaporation of the active organic semiconductor or the synthesis of new organic semiconductor materials. The highest field-effect mobility was obtained for the thermally vacuum-evaporated pentacene TFTs. From the first use of pentacene in organic TFTs in 1992 to 2001, the mobility increased from 2×10^{-3} [9] to 1.5 [10] to 3 [11] $cm^2/Vsec$. These carrier mobilities are similar to or better than those typically obtained with hydrogenated amorphous silicon TFTs, which have found widespread use in active matrix liquid-crystal displays.

With the continuous improvement in device performance, OTFTs need to have stable device operation. However there is an important issue such as threshold voltage shift caused upon applying bias to the gate electrode leading to so called hysteresis behavior. Hysteresis behavior due to bias stress has been reported for transistors based on pentacene, poly(thienylene vinylene) [12-14], a-sexithiophene [15], poly-9,9' dioctyl-fluorene-co-bithiophene (F8T2) and regioregular-polythiophene [16-17]. Several authors have studied to understand the physical origin of this instability and the exact location of the trapped charges. Different dielectric materials and different surface treatment have been studied. Although there have been several studies to explain the hysteresis behavior, there was no report for systematic identification of hysteresis instability by examining hysteresis loop capacitance-voltage (C-V) characteristics of OTFTs.

We have fabricated pentacene OTFTs on glass substrates and measured hysteresis loop capacitance-voltage characteristics to systematically identify the mechanism of hysteresis behavior. In this report, we determine what causes the hysteresis behavior and suggest a possible way of stabilizing the device performance.

2. Exeperiments

Figure 1 shows a schematic cross section of the pentacene organic TFT fabricated in our laboratory. A glass substrate was used as the starting material. The substrate was deposited with a stacked buffer layer of 1000 Å-thick SiNx and 3000 Å-thick SiO_2 in order to prevent the penetration of impurities from the glass substrate into organic TFTs. Both SiNx and SiO_2 were deposited by plasma enhanced chemical vapor deposition (PECVD). Gate electrode, 2000A-thick MoW, was sputter deposited and photo-lithographically patterned on the buffer layer. Following the gate electrode formation, a gate dielectric layer 2000 Å–thick TEOS SiO_2 was deposited by PECVD and patterned. A 2000 Å-thick MoW was then deposited for the source and drain electrode and patterned by wet etching. Instead of using dry etch of MoW, the wet etch process was employed in order not to damage the exposed gate dielectric surface on which the pentacene channel is to be formed. Subsequently pentacene active layer was deposited by thermal evaporation in vacuum. The C-V measurements were carried out on the pentacene organic TFTs with a channel length of 20 μm and a channel width of 500 μm.

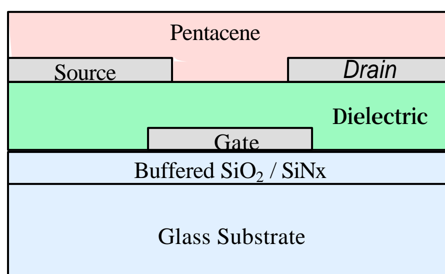

Figure 1. Schematic view of pentacene OTFT fabricated

3. Results and Discussion

Figure 2 shows the room temperature C-V measurements for the gate voltage sweep of $V_G = 0$ V → $V_G = +20$ V → $V_G = -20$ V → $V_G = 0$ V. This curve shows a typical hysteresis behavior that we have seen in many OTFTs. We see a negative shift in the flat band voltage for the negative biasing. The hysteresis shown in Figure 2 can be caused either by mobile charge present in the oxide or by charge-trapping into the oxide. If the mobile ions were the cause of the hysteresis, then the flat band voltage would shift in the positive direction as positively charged mobile ions drift towards the gate during negative gate biasing. (i.e., the arrows in the figure would point in the opposite direction). Thus the above hysteresis is not caused by mobile charges but by charge trapping into the oxide. Generally, during charge trapping in the oxide, electrons or holes from the gate or from the pentacene semiconductor are injected into the oxide, which are subsequently trapped. For a negative bias on the gate, two phenomena can happen: (1) holes from the pentacene semiconductor can be injected into the oxide, giving rise to a negative flat band voltage shift (ΔV_{FB}) and (2) electrons from the gate electrode can be injected into the oxide, giving rise to a positive ΔV_{FB}. On the other hand, for a positive bias, electrons from pentacene can be injected into oxide resulting in positive flat band voltage shift.

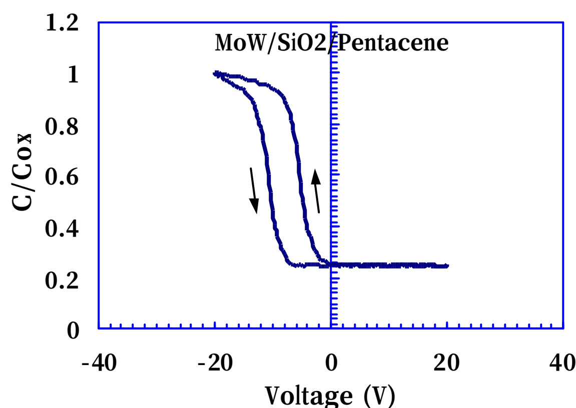

Figure 2. Hysteresis behavior of MoW/SiO_2/Pentacene MOS system. Sweep was made such as $V_G = 0$ V → +20 V → -20 V → 0 V continuously.

To examine what type of carriers are injected and from which interface, we studied the C-V characteristics of MoW/SiO_2/Pentacene MOS system subjected to three consecutive loop sweeps of V_G = +20 V ~ -20 V, +30 V ~ -30 V, +40 V ~ -40 V as shown in Fig. 3. We see in the figure that the flat band voltage ΔV_{FB} shifted successively to more negative for each hysteresis loop during the return sweep of negative gate voltage, $-V_G$, to 0 V. This shows that

holes are injected into the oxide from the pentacene semiconductor (phenomena 1 as mentioned above). We also see that curves for the forward sweep of $+V_G$ → $-V_G$ (i.e., +30 V → -30 V or +40 V → -40 V) are almost identical with the previous curves of return sweep (i.e., -20 V → 0 V or –30 V → 0 V, respectively). This indicates that for positive gate biases, no electrons are injected into the oxide from the pentacene semiconductor.

Figure 4 shows the single forward-sweep C-V characteristics for MoW/SiO_2/Pentacene MOS system. Sweeps were made from positive voltages to negative voltages as V_G= +20 V → -20 V, +30 V → -30 V, +40 V → -40 V, consecutively. Similar to the curves in Figure 3, the flatband voltage shifted to negative for each consecutive sweep with increased gate voltage. Thus these single sweep results also confirm the conclusions reached above which are: (1) for a large positive gate voltage, no electrons are injected from the pentacene semiconductor into the oxide, (2) for a large negative gate voltage, holes are injected from the pentacene semiconductor into the oxide.

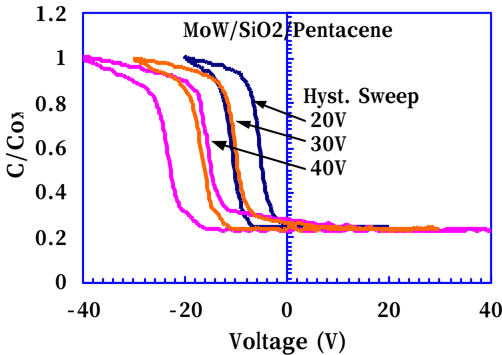

Figure 3 Hysteresis loop C-V characteristics of MoW/SiO_2/Pentacene MOS system. Hysteresis sweep was made such as +20 V ~ -20V, +30 V ~ -30 V, +40 V ~ -40 V consecutively.

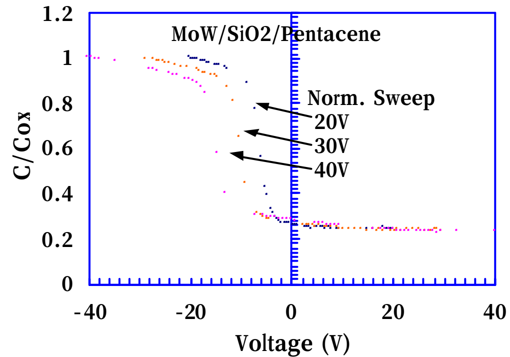

Figure 4. C-V characteristics for MoW/SiO_2/Pentacene MOS system. Positive-to-negative sweep was made such as VG= +20 V → -20 V, +30 V → -30 V, +40 V → -40 V, consecutively.

In Figure 5 we overlaid the curves of Figure 4 (forward sweeps only) onto the curves in Figure 3 (forward-reverse loop sweeps). The curves in Figure 3 and Figure 4 were obtained from two different OTFTs. We see from the Figure 5 that there is a good agreement between the single forward sweep characteristics and forward sweep characteristics of a loop measurement. This confirms that at room temperatures the hysteresis behavior was caused by hole injection into the gate insulator from the pentacene semiconductor for large negative gate voltages, resulting in the negative flat-band voltage shift. Therefore, a kind of surface treatment to build up the higher energy barrier to restrict hole injection from the pentacene semiconductor into the oxide at the interface between the SiO_2 and the pentacene semiconductor may help reduce or eliminate the hysteresis behavior. Surface treatment or insertion of interfacial layer, i.e., hole barrier layer (HBL) could improve the instability or hysteresis behavior in OTFTs.

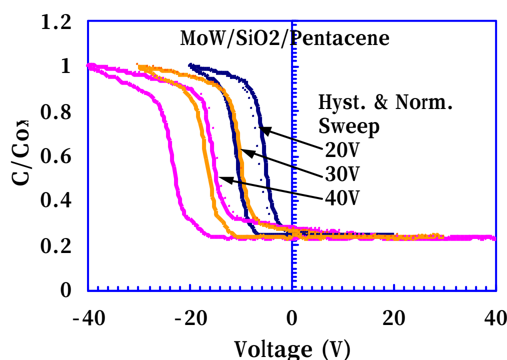

Figure 5. Overlaid plot of the hysteresis loop C-V curves in Figure 3 with the single forward-swept C-V curves in Figure 2.

The C-V characteristics behavior at elevated temperatures was characterized at 30C, 60C, 90C, and 120C as shown in Figure 6. We see from the figure that as the temperature increases, the hysteresis width of C-V characteristics becomes wider. For the reverse sweep of V_G = -20 V → +0 V, as the temperature increases, the magnitudes of the negative flatband voltage shift increases, which implies the hole injection from the pentacene semiconductor into the oxide increases with increase in temperature. Additionally it was found that for the forward V_G sweep of +20 V → -20 V, at elevated temperatures, positive shifts in the flat band voltage are observed and the magnitude of shift increases with an increase in temperature. This implies that at higher temperatures, electron injection from the pentacene semiconductor into the oxide takes place. The electron injection for the room temperature measurement was not seen. We also note from Fig. 6 that even for higher temperatures, a flat band shift related to mobile charges are not noticeable. Also we noticed that the MoW/SiO_2/Pentacene MOS system became unstable and apparently degraded at temperatures of about 100 °C and above.

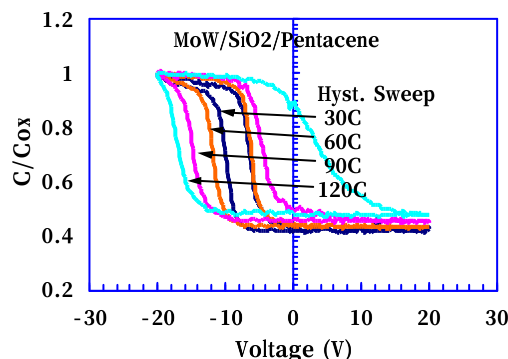

Figure 6. Hysteresis loop C-V characteristics of MoW/SiO_2/Pentacene MOS system measured at elevated temperatures. Hysteresis loop sweep was made between +20 V and –20 V.

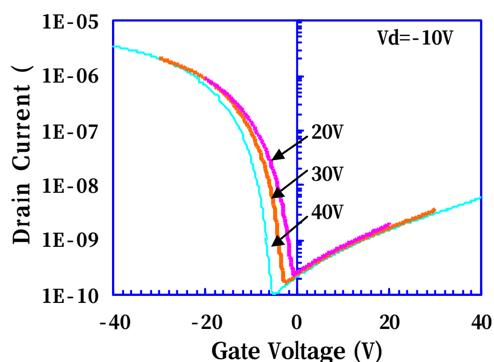

Figure 7. I-V characteristics for MoW/SiO_2/Pentacene MOS system. Positive-to-negative sweep was made such as VG= +20 V → -20 V, +30 V → -30 V, +40 V → -40 V, consecutively.

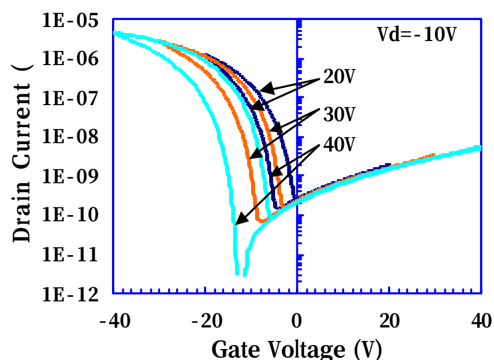

Figure 8. Hysteresis loop I-V characteristics of MoW/SiO_2/Pentacene MOS system. Hysteresis sweep was made such as +20 V ~ -20V, +30 V ~ -30 V, +40 V ~ -40 V consecutively.

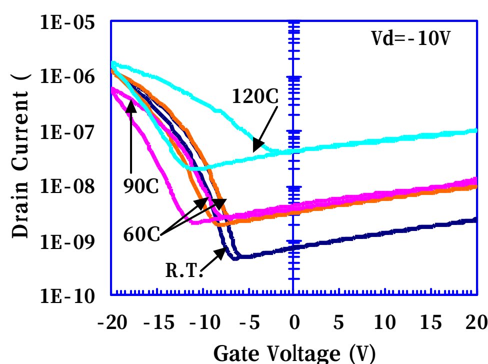

Figure 9. Hysteresis loop I-V characteristics of MoW/SiO_2/Pentacene MOS system measured at elevated temperatures. Hysteresis loop sweep was made between +20 V and –20 V.

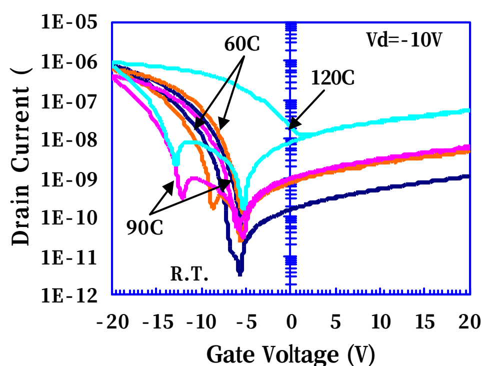

Figure 10. Hysteresis loop I-V characteristics of MoW/SiO_2/Pentacene MOS system measured at elevated temperatures. Hysteresis loop sweep was made between +20 V and –20 V.

4. Conclusions

We have identified the mechanism of hysteresis behavior in pentacene organic TFTs. In efforts to identify the hysteresis behavior, we measured hysteresis loop C-V characteristics on the MoW/SiO_2/Pentacene MOS system at room temperature and elevated temperatures. From the measurement the following conclusions were made: (1) no electron injection into the oxide either from the pentacene semiconductor or from the gate electrode is not seen at room temperature, (2) the holes are injected from the pentacene semiconductor into the oxide for negative gate voltages, causing the flatband voltage shift or hysteresis behavior in C-V characteristics (3) flatband voltage shift due to mobile charge within the oxide isn't observed for large gate voltages even at elevated temperatures, (4) at elevated temperatures, electrons as well as holes are injected into the oxide from the pentacene semiconductor for large positive and negative gate voltages, respectively. (5) MoW/SiO_2/Pentacene MOS system started to be unstable at temperatures of about 100 °C. We believe that some kind of surface treatment or insertion of interfacial layer in between SiO_2 and pentacene semiconductor to increase energy barrier to prohibit holes from being injected into the oxide from the pentacene semiconductor could improve the instability or hysteresis behavior in OTFTs

5. REFERENCES

[1] C.D. Sheraw *et al.,* Tech Dig. – Int. Electron Devices Meet., 2000, 619.

[2] G.H. Gelinck, T.C.T. Geuns, and D.M. de Leeuw, Appl. Phys. Lett. 77, 1487 (2000)

[3] B.K. Crone, A. Dodabalapur, R. Sarpeshkar, R.W. Filas, Y.Y. Lin, Z. Bao, J.H. O'Neill, W.Li, and H.E. Katz, J. Appli. Phys., 89, 5125 (2001)

[4] J.H. Schon and C. Kloc, Appl. Phys. Lett., 79, 4043 (2001)

[5] C.D. Sheraw et al., Appl. Phys. Lett., 80, 1088 (2002)

[6] H.E. A. Huitema, G.H. Gelinck, J.B.P.H. van der Putten, K.E. Kuijk, K.M. Hart, E. Cantatore, and D.M. de Leeuw, Adv. Mater 14, 1201 (2002)

[7] P. Mach, S.J. Rodriguez, R. Nortrup, P. Wiltzius, and J.A. Rogers, Appl. Phys. Lett., 78, 3592 (2001)

[8] J.A. Rogers et al., Proc. Natl. Acad. Sci. U.S.A. 98, 4835 (2001)

[9] G. Horowitz, X. Peng, D. Fichou, F. Garnier, Role of the semiconductor/insulator interface in the characteristics of π-conjugated-oligomer-based thin-film transistors, Synth Met 51:419-424, 1992

[10] Y.Y. Lin, D.J. Gundlach, S. Nelson, T.N. Jackson, Stacked pentacene layer organic thin-film transistors with improved characteristics, IEEE Electron device Lett., 18:606-608, 1997

[11] J.H. Schon and C. Kloc, Appl. Phys. Lett., 79, 4043 (2001)

[12] A. R. Brown, C. P. Jarret, D. M. de Leeuw, and M. Matters, Synth. Met. 88, 37 (1997).

[13] M. Matters, D. M. de Leeuw, P. T. Herwig, and A. R. Brown, Synth. Met. 102, 998 (1999).

[14] S. J. Zilker, C. Detchverry, E. Cantatore, and D. M. de Leeuw, Appl. Phys. Lett. 79, 1124 (2001).

[15] W. A Schoonveld, J. B. Oosting, J. Vrijmoeth, and T. M. Klapwijk, Synth. Met. 101, 608 (1999).

[16] A. Salleo and R. A. Street, J. Appl. Phys. 94, 471 (2003).

[17] R. A. Street, A. Salleo, and M. Chabinc, Phys. Rev. B 68, 085316 (2003).