

Electrical performance and contact resistance with the substrate temperature in the pentacene organic thin-film transistors

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Abstract

Bottom contact pentacene organic thin-film transistors are fabricated at three different substrate temperatures, 70 °C, 80 °C and 90 °C. The maximum effective mobility was obtained at 80 °C. The contact resistance was extracted by applying two different methods, TLM method and channel-resistance method, and the value shows the minimum at 80 °C, which is thought to be the important reason for the best performance.

1. Introduction

Organic thin-film transistors (OTFTs) have many applications as a driving device for the flexible display [1], RFID tag [2], [4] or smart card. Especially, the evaporated pentacene is attractive as a semiconductor active layer due to its high electrical performances [3-4]. However, the evaporation method is affected by many process variables and the substrate temperature is one of them.

Although it has been reported that there is an optimal substrate temperature in many previous results [5-6], the exact reason is not clear yet. In this paper, the effect of the substrate temperature for the electrical performance was analyzed from the viewpoint of the contact resistance.

2. Experiment and result

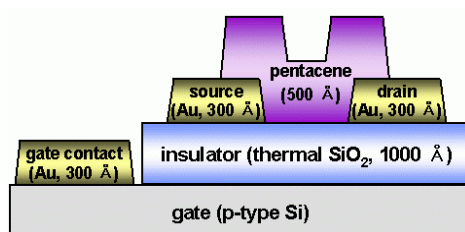


Fig. 1. Device structure of the fabricated bottom contact organic thin-film transistors (OTFTs).

The pentacene OTFT devices fabricated in this work have the bottom contact configuration shown in Fig. 1. For convenience, the devices were fabricated on the p-type silicon substrate. The Si substrate serves as a common gate and the thermally grown SiO₂ was used as a gate insulator. The conventional photolithography, evaporation of gold and lift-off process was carried out sequentially to define the source and drain. The device was completed by the thermal evaporation of pentacene at the high vacuum ambient of about 10⁻⁸ Torr. Pentacene was patterned through an aligned shadow mask. The substrate temperature during the pentacene deposition was split to three different conditions around optimum point, i.e., 70 °C, 80 °C and 90 °C [7]. The deposition rate was sustained at 0.5~1.1 Å/sec. The electrical characteristic was measured in the atmosphere without passivation using a HP4156C semiconductor parameter analyzer.

Fig. 2 illustrates the typical transfer curves of the OTFT that is evaporated at 80 °C of substrate temperature. From the transfer characteristics, the electrical parameters such as threshold voltage and mobility are extracted at the linear and saturation region as shown in Fig. 3.

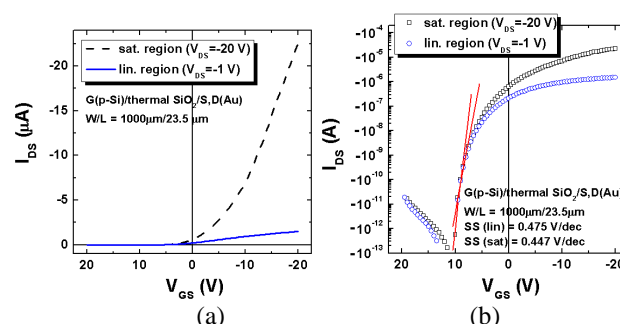


Fig. 2. Typical transfer characteristics in (a) the linear scale and (b) log scale for the devices fabricated at the substrate temperature of 80 °C.

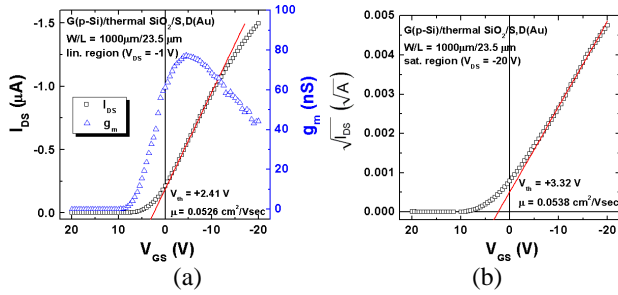


Fig. 3. Extraction of the threshold voltage and effective mobility at the (a) linear region ($V_{DS} = -1$ V) and (b) saturation region ($V_{DS} = -20$ V).

Fig. 4 depicts the mobility and threshold voltage distribution of the measured devices with various channel lengths ranging from 3 μm to 30 μm . The mobility value is reducing with the channel length decrease due to the increase of the contact resistance [8] and the threshold voltage value is increasing probably due to the short channel effect [9]. By applying the same procedure, the mobility and threshold voltages are extracted for the devices fabricated at different substrate temperature, 70 $^\circ\text{C}$ and 90 $^\circ\text{C}$.

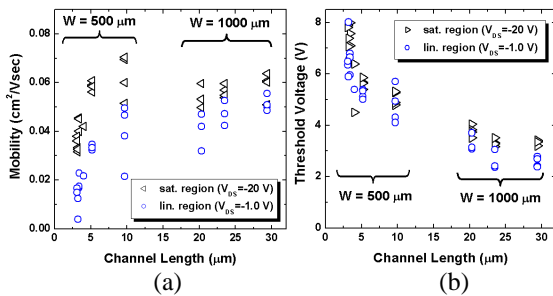


Fig. 4. Extracted (a) mobility and (b) threshold voltage distribution for the devices with various channel lengths.

3. Discussion

Fig. 5 compares the saturation mobility with the substrate temperature when the channel length is 5 and 25 μm . The highest mobility was obtained at 80 $^\circ\text{C}$ and the trend is consistent with the previous result [7]. The threshold voltage and subthreshold slope do not show any special trends as a function of the substrate temperature.

The reason for the highest mobility at the 80 $^\circ\text{C}$ is analyzed by extracting the contact resistance applying the two different methods, TLM (Transmission Line Method or Transfer Length Method) [6] and channel-resistance method [10].

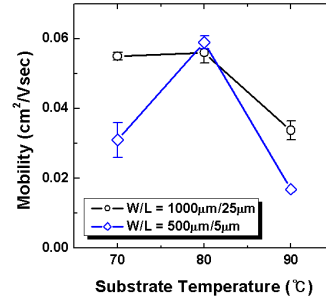


Fig. 5. Mobility with the substrate temperature.

Fig. 6 shows the TLM measurement results for the devices fabricated at the substrate temperature of 80 $^\circ\text{C}$. The I-V curves are not linear possibly due to the lateral-field dependent mobility characteristic [11]. The total resistance was extracted when the voltage difference is equal to 0 V. The total resistance with the various channel length is drawn in Fig. 6 (b).

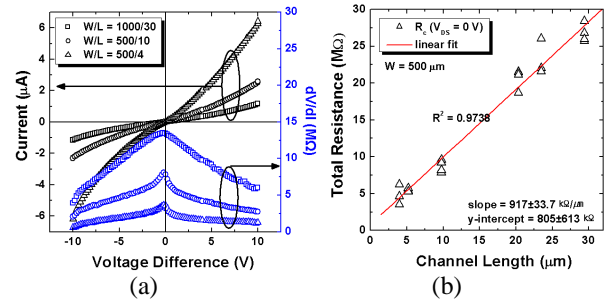


Fig. 6. (a) Current-voltage characteristic by the TLM measurement. (b) Total resistance plot with the various channel lengths.

| sub. temp. (dep. rate) | ① 70 $^\circ\text{C}$ (0.5 $\text{\AA}/\text{sec}$) | ② 80 $^\circ\text{C}$ (1.1 $\text{\AA}/\text{sec}$) | ③ 90 $^\circ\text{C}$ (1 $\text{\AA}/\text{sec}$) |
|--|---|---|---|
| effective mobility ($L=25\mu\text{m}$, sat. region) | 0.055 ± 0.001 | 0.056 ± 0.003 | 0.036 ± 0.001 |
| effective mobility ($L=5\mu\text{m}$, sat. region) | 0.031 ± 0.005 | 0.059 ± 0.002 | 0.0169 |
| sheet resistance ($V_{DS}=0$ V; unit: $\text{K}\Omega/\square$) | 321 ± 14 | 459 ± 17 | 782 ± 47 |
| contact resistance (TLM method, $V_{GS}=0$ V, $W=1$ cm; unit: $\text{K}\Omega$) | 112 ± 23 | 40 ± 31 | 472 ± 96 |

Table 1. Extracted sheet resistance, and contact resistance for the devices fabricated at different substrate temperatures by applying the TLM method.

From the intercept for the vertical axis and the slope of the straight regression line, the contact resistance and sheet resistance can be extracted, respectively. Table. 1 summarizes the sheet resistance and contact resistance with the substrate temperature extracted by applying the TLM method. The minimum contact resistance is observed at the 80 $^\circ\text{C}$ of the substrate temperature.

For the comparison, another method, i.e. channel-resistance method [10] was applied to extract the contact resistance. The total resistance was calculated from the I_{DS} - V_{GS} curve at the linear region with the same gate overdrive $V_{GS}-V_{th}$. Fig. 7 describes the calculated total resistance plot with the various channel lengths when the substrate temperature during pentacene deposition was 80 °C. The vertical coordinate of the common intercept determines the contact resistance.

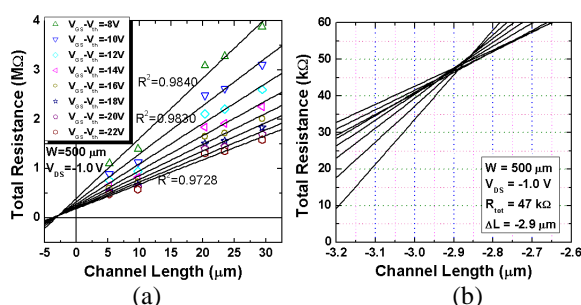


Fig. 7. (a) Total resistance versus channel length for the same gate overdrives applying the channel-resistance method and (b) its magnified version around the intersections.

Applying the same method, the contact resistances are extracted for the other substrate temperatures, 70 °C and 90 °C during pentacene deposition. The results are summarized in Table 2. From Table 2, the contact resistance is minimum when the pentacene is deposited at the 80 °C of the substrate temperature, which is consistent with the results in Table. 1.

| sub. temp. (dep. rate) | ① 70 °C (0.5 Å/sec) | ② 80 °C (1.1 Å/sec) | ③ 90 °C (1 Å/sec) |
|--|------------------------|------------------------|----------------------|
| effective mobility ($L=25 \mu\text{m}$, sat. region) | 0.055 ± 0.001 | 0.056 ± 0.003 | 0.036 ± 0.001 |
| effective mobility ($L=5 \mu\text{m}$, sat. region) | 0.031 ± 0.005 | 0.059 ± 0.002 | 0.0169 |
| contact resistance (channel-resistance method, $V_{GS}=1V$, $W=1 \text{ cm}$, unit: Ω) | 30 | 2.4 | ~100 |

Table 2. Contact resistance with the substrate temperature extracted by the channel-resistance method.

Therefore, it can be inferred that the lowest contact resistance at the condition of 80 °C is the important reason for the highest mobility though it cannot be fully understood yet why the contact resistance is reduced to minimum at that temperature.

5. Conclusion

The fabricated pentacene OTFTs have the best electrical performance at 80 °C of the substrate

temperature during pentacene deposition. The contact resistance extracted by the two different extraction methods shows the minimum value at that temperature, which is one of the important reason for the best electrical performance.

6. Acknowledgements

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7. References

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