# Hybrid Insulator Organic Thin Film Transistors With Improved Mobility Characteristics

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## Abstract

*Hybrid insulator pentacene thin film transistors (TFTs) were fabricated with thermally grown oxide and cross-linked polyvinylalcohol (PVA) including surface treatment by dilute ploymethylmethacrylate (PMMA) layers on $n^+$ doped silicon wafer. Through the optimization of $SiO_2$ layer thickness in hybrid insulator structure, carrier mobility was increased to above 35 times than that of the TFT only with the gate insulator of $SiO_2$ at the same transverse electric field. The carrier mobility of 1.80 $cm^2$/V-s, subthreshold swing of 1.81 V/decade, and $I_{on}$/ $I_{off}$ current ratio > 1.10 × $10^5$ were obtained at low bias (less than -30 V) condition. The result is one of the best reported performances of pentacne TFTs with hybrid insulator including cross-linked PVA material at low voltage operation.*

## 1. Introduction

In recent years, a lot of efforts have been attempted to improve the performances of organic thin film transistors (OTFTs) [1], [2] for many applications such as flexible circuits [3], radio-frequency identification tags [4] and sensors [5]. Therefore, the high carrier mobility of devices is also demanded for these applications. One of the effective approaches to enhance the electrical characteristics of OTFTs is to select gate dielectric layer with various materials [6].

In this paper, we newly propose the hybrid insulator structure with cross-linked PVA, $SiO_2$ and PMMA layer for the transistors to increase carrier mobility of TFTs and merge the influences of each insulator.

Among the various gate insulator materials, cross-linked PVA was adopted as a polymer gate insulator because of its high-k characteristics [7], photosensitivity [8] and good surface alignment effect [8]. Additionally, the surface treatment of cross-linked

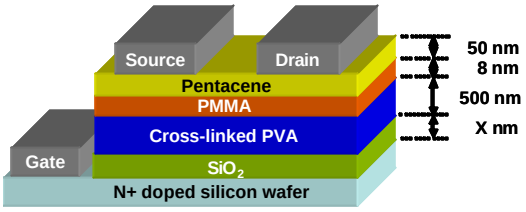


Fig. 1. Device structure of hybrid insulator OTFTs with $SiO_2$, cross-linked PVA and PMMA layers. W/L = 1000/25 (㎛).

PVA was performed by coating of PMMA solution to modify the surface state of gate dielectric layer. It is expected to provide a similar termination to silicon single crystals on which hydrocarbons are chemisorbed [9] to reduce heterogeneous nucleation facilitating grain growth [9]. Finally, $SiO_2$ was adopted as a barrier layer to reduce carrier injection from gate electrodes and enhance the saturation characteristics in hybrid structure.

## 2. Device Fabrication

The top contact transistors were fabricated on $n^+$ doped silicon wafers which were used as gate electrodes. The silicon wafers were thermally oxidized to obtain to be 8, 40, and 100 ㎚ thickness of $SiO_2$ which serve as the inorganic gate dielectrics. The PVA solution with ammonium dichromate photosensitizer was spin-coated on the $SiO_2$ layer to serve as 500 ㎚ thick polymer gate dielectric layer. The coated PVA was exposed with UV light and heated at 110 ℃ for 5 hours in a convection oven to define gate insulator and to make cross-linking PVA's molecules, respectively. The dielectric constant of cross-linked PVA was measured to be e = 5.1 at 10 kHz frequency.

For the surface modification, 8 ㎚ thick PMMA

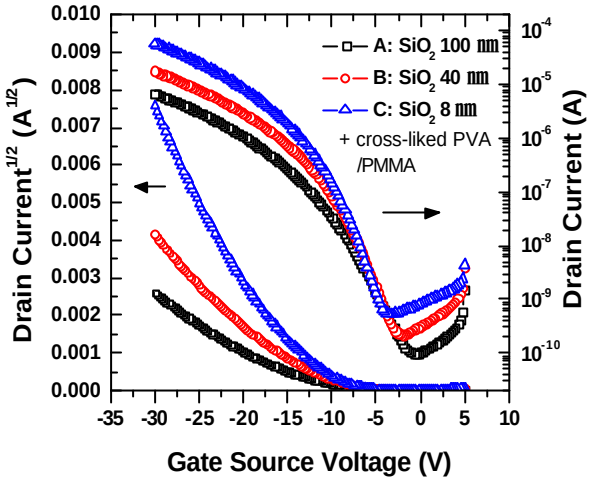


Fig. 2. Electrical transfer characteristics of split hybrid insulator OTFTs: sample A = $SiO_2$ (100 nm)/PVA (500 nm)/PMMA (8nm), sample B = $SiO_2$ (40 nm)/PVA (500 nm)/PMMA (8nm), and sample C = $SiO_2$ (8 nm)/PVA (500 nm)/PMMA (8nm).

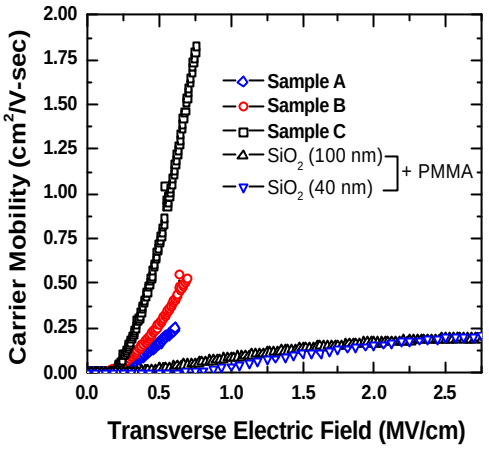


Fig. 3. Carrier mobility versus vertical electric field for split hybrid insulator devices ($SiO_2$ (X nm)/PVA (500 nm)/PMMA (10nm)) and PMMA treated $SiO_2$ insulator devices (40 and 100nm) in saturation regime. The thickness ratio of cross-linked PVA vs. $SiO_2$ in hybrid insulator devices: sample A = 5:1, B = 12.5:1, and C = 62.5:1 for 100, 40, and 8 nm $SiO_2$ layer, respectively.

layer was formed onto the cross-linked PVA layer by spin-coating process and it was baked at 110 °C for 30 minutes. In a final step, 50 nm thick pentacene films were deposited using a thermal evaporation system, keeping the substrate temperature of 80 °C and deposition rates in the range of 0.5-1.0 Å/s. Afterward, gold was thermally evaporated on top of the pentacene layer using shadow masks giving transistors with 25 μm channel length and 1000 μm width. The cross-sectional illustration of the device is schematically shown in Fig. 1.

## 3. Electrical Characteristics and Discussion

Fig. 2 shows the transfer characteristics of our hybrid insulator pentacene TFTs under the three different gate dielectric conditions. For the same level sweeps and low voltage operation in saturation regime, the drain voltage was held constant at -30 V to the all devices. The carrier mobility and threshold voltage were calculated from the slope of the plot of $|I_D|^{1/2}$ versus $V_{GS}$ at -30 V of gate voltage in Fig. 2. The extracted values of electrical parameters for the devices are summarized in Table 1. As shown in the insets of Fig. 2 and Table 1, noticeably improved drain current and carrier mobility was inspected according the reduction of $SiO_2$ layer thickness in hybrid insulator.

In low bias condition (less than -30V), the pronounced result was extracted from the sample A (8 nm $SiO_2$ + 500nm cross-linked PVA + 8 nm PMMA): the carrier mobility of 1.80 $cm^2/V$-s, subthreshold swing of 1.81 V/decade, and $I_{on}/ I_{off}$ current ratio > $1.10 \times 10^5$ were obtained. Since the carrier mobility of OTFTs has dependency by gate bias [10], the result is one of the best results of hybrid insulator pentacene TFTs including cross-linked PVA gate dielectric material at low voltage operation.

To further study of cross-linked PVA effect and equivalent comparison between the gate dielectric condition and carrier mobility, we have inspected the correlation of carrier mobility vs. transverse electric field for the same structured samples shown in Table. 1 and the two kinds of devices with PMMA treated 40, 100 nm $SiO_2$ gate dielectric layers. The compared result was shown in Fig. 3.

From this figure, 0.238, 0.402, 1.139 $cm^2/V$-sec of carrier mobility was extracted at 0.6 MV/cm transverse electric field in hybrid insulator devices which correspond to the thickness ratio of cross-linked PVA vs. $SiO_2$ of 5:1 ($T_{ox}$ = 100 nm), 12.5:1 ($T_{ox}$ = 40 nm), and 62.5:1 ($T_{ox}$ = 8 nm) in hybrid insulator, respectively. The optimum-device sample A shows 35 times larger mobility than that of the TFTs only with

the PMMA treated $SiO_2$ (100 nm) gate insulator at the same transverse electrical field by using the hybrid insulator which has 62.5 times larger cross-linked PVA portion than $SiO_2$ thickness. Whereas, a slight mobility change is occurred in the devices with $SiO_2$ insulator (40 and 100nm). Therefore, these results prove that the effect of cross-linked PVA gate dielectric layer which greatly improve carrier mobility at the same electric field condition in hybrid insulator OTFTs.

## 4. Conclusion

In this paper, we proposed a new hybrid insulator structure with thermally grown oxide and cross-linked PVA layer including PMMA treatment to increase carrier mobility of pentacene TFTs. Through the optimization of hybrid insulator by the reduction of $SiO_2$ layer thickness, we increased the carrier mobility of devices to above 35 times of magnitude than that of $SiO_2$ insulator devices. Additionally, the effect of cross-linked PVA for increasing carrier mobility was fairly proved using the comparison of carrier mobility vs. transverse electric field for the devices which have different thickness ratio of cross-linked PVA and $SiO_2$ layer in hybrid insulator.

From the optimum devices with $SiO_2$ (8 nm) + cross-linked PVA (500nm) + PMMA (8 nm) hybrid insulator structure, The carrier mobility of 1.80 $cm^2/V$ s, subthreshold swing of 1.81 V/decade, and $I_{on}/I_{off}$ current ratio > $1.10 \times 10^5$ were obtained at low bias (less than -30 V) condition.

Table. 1. Summary of the electrical parameters for hybri insulator OTFTs according to the changed thickness rati of oxide and cross-linked PVA layer by the reduction o $SiO_2$ thickness in hybrid insulator (X nm $SiO_2$/500 nm cross-linked PVA/8 nm PMMA).

| Ratio of cross-linked PVA vs. $SiO_2$ | $T_{ox}$ (nm) | $\mu_{eff}$ ($cm^2$/V-s) | $V_{th}$ (V) | $I_{on}/I_{off}$ ratio | SS (V/dec) |
|---|---|---|---|---|---|
| 5:1 | 100 | 0.25 | - 15.2 | $6.9 \times 10^4$ | 2.92 |
| 12.5:1 | 40 | 0.53 | - 15.0 | $8.0 \times 10^4$ | 2.28 |
| 62.5:1 | 8 | 1.80 | - 14.9 | $1.1 \times 10^5$ | 1.81 |

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