Effects of Peripheral Pentacene Region on C-V Characteristics of Metal-Oxide-Pentacene Capacitor Structure

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Abstract
Peripheral pentacene region gives a significant influence on C-V characteristics of metal-oxide-pentacene capacitor structure. When the gate voltage goes toward negative, the effect of peripheral pentacene region becomes larger. Remaining gate DC bias constant and changing small signal frequency, the capacitance of peripheral pentacene changes along with frequency so that the total capacitance value also changes. The influence of peripheral pentacene region should be removed to measure accurate C-V characteristics, because it is hard to take into account the effect of the region quantitatively. After removing the influence of peripheral pentacene region, acceptor concentration, flat band voltage and depletion width of pentacene thin film are extracted from an accurate C-V curve as 1.58×10^{17} *cm*$^{-3}$*, -1.54 V and 39.4 nm, respectively.*

1. Introduction
Among various organic semiconductors, pentacene has been widely used in OTFTs as an organic semiconducting layer due to its high field effect mobility. As active researches has been focused on the performance improvement of OTFTs, intrinsic properties of pentacene thin films has seldom been investigated. Moreover, simple MOS capacitor [1, 3] is relatively less studied compared to OTFTs, though it can give a lot of information about pentacene thin film. When pentacene MOS structure being investigated, peripheral pentacene region is known to affect C-V characteristics [1], and the value of capacitance changes with different measuring frequency [1]. However, it is difficult to fabricate pentacene capacitor without peripheral pentacene region because accurate alignment is hard when using shadow masks to define pentacene or metal layers. From this point of view, the effect of peripheral pentacene region on C-V characteristics was examined in this paper. In addition, with simple technique to remove peripheral pentacene region, accurate C-V curve and pentacene thin film parameters were obtained.

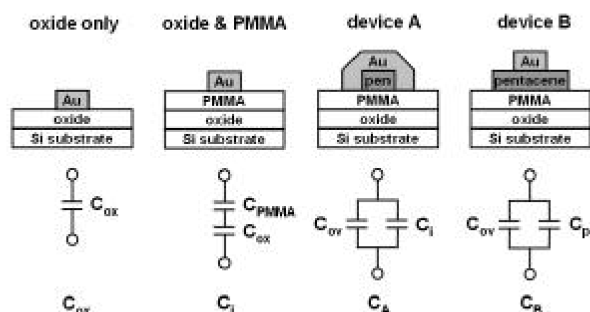

Fig 1. The fabricated devices. Pentacene thin films and gold electrodes are patterned with metal shadow masks.

2. Experiments
Heavily doped silicon wafer with sheet resistance of 10 Ω/□ was used as a gate electrode. 35 nm-thick-oxide was thermally grown and used as a gate insulator. 9:1 dilute PMMA was spin-coated on the SiO_2 to improve pentacene ordering and grain size [2]. Pentacene film of 50 nm thickness was thermally evaporated through a metal shadow mask at 80° C of substrate temperature. 50 nm-thick-film of gold was e-gun evaporated on the pentacene film through a metal shadow mask.

Fig 1 shows the fabricated devices. To evaluate the effect of PMMA treatment on C-V characteristics, two kinds of simple MOS-C devices are prepared without any pentacene layer. In device A, the pentacene layer is covered by a larger gold electrode, so there exist no peripheral pentacene region even if

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small misalignment occurs between two shadow masks. On the other hand, the pentacene layer is larger than the gold electrode in device B, so that peripheral pentacene region is always made. In both of device A and B, sizes of overlapping region between pentacene and gold are always the same in spite of small misalignment. To prevent variation among devices, device A, device B and PMMA treated simple capacitor without pentacene are made simultaneously on a same substrate.

Simple circuit model is also shown in Fig 1. PMMA treated oxide capacitance (C_i) can be thought of coupling of C_{ox} and C_{PMMA} in series. For the case of device A, total capacitance is sum of pentacene-gold overlapping capacitance (C_{ov}) and insulator capacitance (C_i) coupled in parallel. Because C_i can be measured easily, accurate C_{ov} can be obtained by simple calculation. For device B, total capacitance is composed of C_{ov} and peripheral pentacene region capacitance (C_p) connected in parallel. Assuming that C_{ov} in device A and device B are the same, C_p can be obtained from simple arithmetic, too.

All C-V characteristics were measured in air with HP4284A LCR meter. Small signal frequency ranges from 100 Hz to 10 kHz, and the amplitude is varied from 1 mV to 1 V depending on measurement condition.

3. Results and Discussion

3.1 Effect of peripheral pentacene region on C-V characteristics

Fig 2 shows difference in C-V characteristics between two capacitor structures; device A and device B. Fig 2(a) and 2(b) are as measured data at frequency 10 kHz. From Fig 2(a), C_{ov} can be calculated accurately, and is depicted in Fig 2(c). The shape of this curve is similar to typical p-type silicon MOS-C high frequency C-V characteristics. The capacitance at V_G=-10 V and measured C_i meet with 99 % accuracy. This result indicates that hole accumulation layer is formed inside the pentacene thin film, and the layer responds to the small AC signal very well just like the gold electrode. A more detailed analysis of this curve will be given later in this paper.

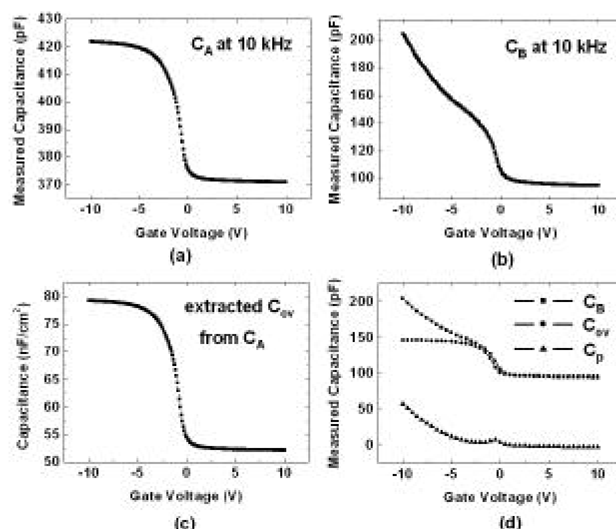

Fig 2. (a) As measured capacitance in device A (C_{ov} + C_i) (b) As measured capacitance in device B (C_{ov} + C_p) (c) Extracted C_{ov} per unit area from measured capacitance C_A (d) Seperated C_p from C_B. When there is peripheral pentacene region, C_p has a significant influence on the total capacitance value.

Using the curves in Fig 2(b) and 2(c), C_p can be calculated as described previously. The result is depicted in Fig 2(d). In this graph, capacitance of device B is separated into two components. One is C_{ov} which is attained from Fig 2(c), and the other is C_p, the difference between the total capacitance and C_{ov}. As shown in Fig 2(d), as the gate bias goes toward negative, the value of C_p is increasing. This indicates that holes can respond to the gate bias even in the peripheral pentacene region. Moreover, as the gate bias becomes larger, more holes can be induced in peripheral pentacene region, so the measured C_p increases.

3.2 Frequency dependency of C-V characteristics

Until now, measuring frequency is fixed at 10 kHz. But, different from silicon MOS-C, it is known that measuring frequency in organic MOS-C structure can change C-V characteristics [1]. Thus, effect of peripheral pentacene region according to measuring frequency should be investigated at frequencies other than 10 kHz.

At first, it is necessary to check the effect of PMMA surface treatment on the oxide capacitance. In Fig 3(a), we compared C_{ox} and C_i where all the data is

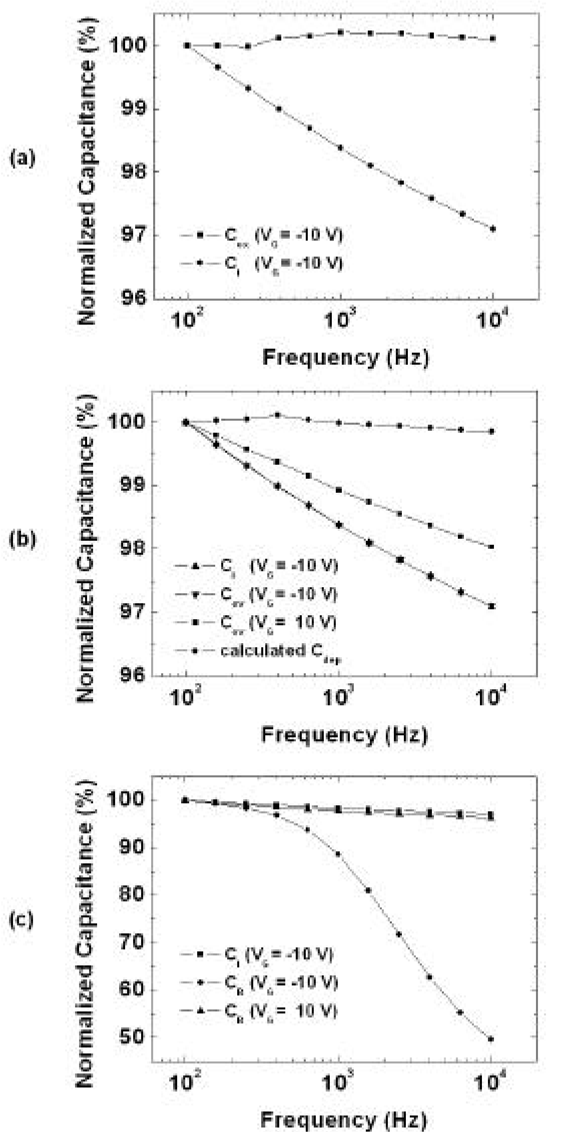

Fig 3. (a) C_i slightly decreases as frequency increases (b) When no peripheral region exist (device A), measured capacitance coincide with case B with 97 % accuracy at V_G=-10 V, and calculated C_{dep} is almost constant. (c) If there is peripheral region, capacitance at V_G=-10 V changes significantly.

normalized using the data at 100 Hz as a reference (100 %). As already known, C_{ox} appears not dependent on frequency. But, the capacitance of PMMA-treated device (C_i) decreases slightly as frequency increases. This result is attributed to the frequency dependency of dielectric constant of PMMA layer.

In Fig 3(b), device A is examined regarding the C_i curve in Fig 3(a) as a reference. With V_G=-10 V, the measured C_{ov} coincide to the C_i within 99% accuracy regardless of frequencies. This means that high negative gate voltage can make enough hole accumulation layer at all frequency to respond to the small gate voltage variation. In the another case at V_G=10 V, measured capacitor can be thought as pentacene depletion capacitor (C_{dep}) and C_i connected in series. From the figure, this capacitor also shows slight frequency dependent characteristics. Comparing V_G=10 V data with V_G=-10 V curve, C_{dep} can be obtained as shown in Fig 3(b), and different from other capacitance it shows almost no frequency dependency.

In Fig 3(c), the fixed-bias capacitance of device B with different frequency is compared to the C_i curve in Fig 3(a). Different from device A, capacitance at V_G=-10 V is strongly dependent on the frequency when peripheral pentacene region exists. At 10 kHz, measured capacitance is only 50 % as much as the value at 100 Hz. But when V_G=10 V, no significant change according to the frequency can be found.

3.3 Pentacene thin film properties extracted from C-V characteristics

As shown above, it is hard to take into account the effect of peripheral pentacene region quantitatively. As a result, all peripheral pentacene region should be removed to get and analyze accurate C-V curve.

Generally, silicon device theory is not applicable to the organic devices. But at least in the depletion regime, we can think that the Poisson's equation is applicable, because it is related to only the fixed ion in the depletion region. Using Poisson's equation and depletion approximation, we can derive the capacitance and gate voltage relation when the device is under depletion regime as below.

$$\frac{1}{C^2} = \frac{1}{{C_{ox}}^2} + \frac{2}{\varepsilon_{pen} q N_A}(V_G - V_{FB})$$

And for the case of depletion capacitor, the below equation can be used to roughly evaluate the depletion width. And as shown previously, this depletion width has no dependency on frequency.

$$C_{dep} = \frac{\varepsilon_{pen}}{W_{dm}}$$

Here, the extracted C_{ov} curve in Fig 2(c) was used for these analyses. In table 1, extracted parameters are

summarized. Pentacene dielectric constant used here was 6.7 following [3].

parameters	value
acceptor concentration (N_A)	1.58×10^{17} cm^{-3}
flat band voltage (V_{FB})	-1.54 V
depletion width (W_{dm})	39.4 nm

Table 1. parameters extracted from C-V curve when there is no peripheral pentacene region

4. Conclusions

The effects of peripheral pentacene region on C-V characteristics were examined using simple metal-oxide-pentacene capacitor structure. When there is peripheral pentacene region, measured capacitance changes significantly, especially with changing gate voltage as well as changing measurement frequency. After removing peripheral pentacene region, C-V characteristics do not show frequency dependency. From an exact C-V curve, acceptor concentration, flat band voltage and depletion width of pentacene thin film are extracted as 1.58×10^{17} cm^{-3}, -1.54 V and 39.4 nm respectively.

5. Acknowledgements

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6. References

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