Single-Crystal Silicon Thin-Film Transistor on Transparent Substrates

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Abstract

Single-crystal silicon thin films on glass (SOG) and on fused-quartz (SOQ) were prepared using wafer bonding and hydrogen-induced layer transfer. Thin-film transistors (TFTs) were subsequently fabricated. The high-temperature processed SOQ TFTs show better device performance than the low-temperature processed SOG TFTs. Tensile and compressive strain was measured respectively on SOQ and SOG. Consistent with the tensile strain, enhanced electron effective mobility was measured on the SOQ TFTs.

Keywords: transparent substrate, glass, quartz, ion cutting, layer transfer, single-crystalline silicon, thin-film transistor

1. Introduction

Electro-optical systems requiring transparent substrates, such as active-matrix flat-panel displays for personal digital assistant, digital camera and mobile phone, etc. are currently realized using thin-film electronic devices built on amorphous or polycrystalline semiconductor, such as silicon (Si). The performance of these systems, measured in terms of speed, power consumption, resolution and level of integration could be greatly enhanced if thin films of single-crystalline material were available. However, it is difficult to form single-crystalline silicon (c-Si) directly on amorphous transparent substrates using conventional deposition techniques.

Wafer bonding is an effective method for integrating materials with different crystal structures [1-11]. Offering both process simplicity and better film uniformity, hydrogen-induced "ion-cutting" [7-11] is a powerful technique for the subsequent transfer of the c-Si film. Applications to both c-Si on glass (SOG) [1-3] and on quartz (SOQ) [4-9] have been reported. SOQ offers potentially the best device performance, because of its compatibility with high temperature processing. However, the large difference between the coefficients of thermal expansion (CTE) of Si and fused quartz complicates the bonding and film transfer process.

Preparation of SOG and SOQ is presently reported. After the bonding of hydrogen-implanted Si wafers to glass or quartz substrates, thin films of Si were thermally exfoliated and transferred to glass but mechanical exfoliated and transferred to quartz. Thin-film transistors (TFTs) subsequently fabricated on these substrates were characterized. The respective highest processing temperatures for the SOG and SOQ TFTs were 620˚C and 1000˚C.

2. SOG and SOQ Preparation

Shown in Figure 1 is the schematic illustration of the wafer bonding and c-Si film transfer process.

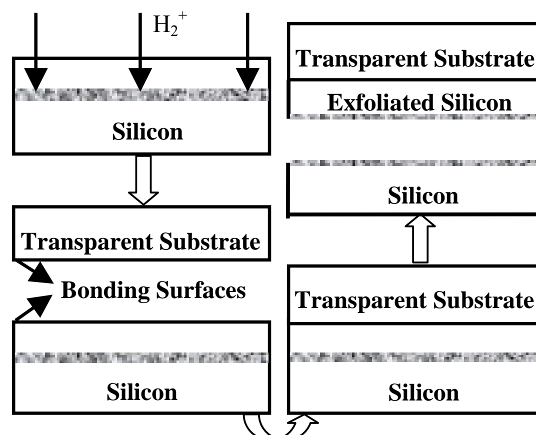

Figure 1. Schematics of the layer-transfer process.

P-type, 1-2Ωcm, (100)-oriented and hydrogen-implanted Si wafers were used as the starting substrates. Prior to wafer bonding and accompanied by the corresponding Si wafers, glass and quartz wafers were treated respectively in an oxygen or argon plasma. Bonded pairs were subsequently

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annealed at 250˚C to increase the bonding strength. Due to the significant difference between the CTEs of quartz and Si, a more gradual temperature ramp to reach the annealing temperature was selected for SOQ. SOG was obtained by thermally-induced exfoliation at ~450°C. SOQ was obtained by blade-assisted, mechanically-induced exfoliation at room temperature. The as-transferred SOG and SOQ are shown in Figure 2.

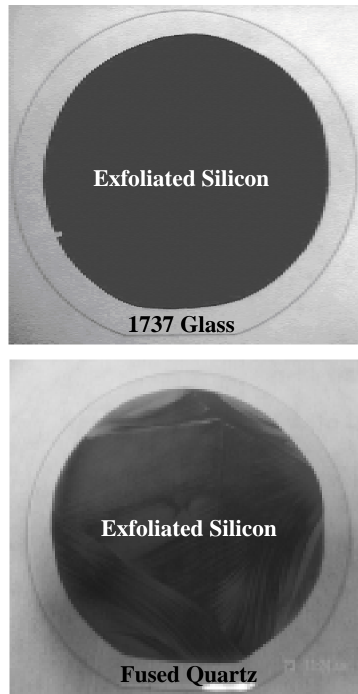

Figure 2. As-transferred SOG and SOQ wafers.

Shown in Figure 3 are micrographs of the SOG bonding interface obtained using cross-sectional transmission-electron microscopy (XTEM). Crystal defects can be observed on the exfoliated surface.

Chemical-mechanical polishing was carried out to remove surface defects and reduce roughness. In order to recover the original p-type conductivity of the Si wafers [11] and to further enhance the bonding strength, the substrates were annealed in nitrogen. The thermal schedule for SOQ was 600˚C for 60 minutes followed by 1000˚C for 60 minutes; that for SOG was 630˚C for 100 hours. The extended annealing time was applied to SOG to reduce substrate deformation during device fabrication by "pre-shrinking" the glass. For SOQ, an additional thermal oxidation was performed to adjust the Si film thickness. The final thickness of SOG and SOQ is ~130-150nm and ~100nm, respectively.

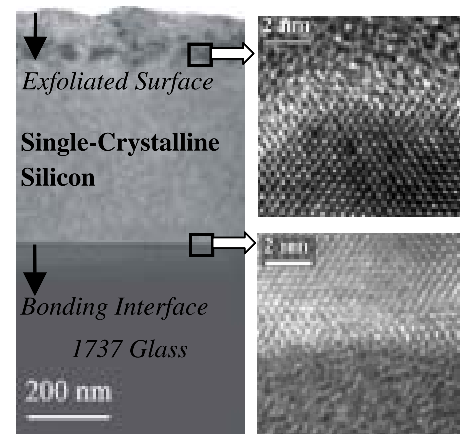

Figure 3. XTEM micrograph of bonding interface and exfoliated surface.

3. Device Fabrication

The device fabrication flow is outlined in Figure 4. The process started with a phosphorous implantation to define the n-well regions where the p-type devices would be built. The respective gate dielectric was low-pressure chemical vapor deposited (LPCVD) low temperature oxide (LTO) at 420˚C and thermally-grown oxide at 950˚C for SOG and SOQ TFTs. The respective dopant activation schedules were 550˚C for 8 hours and 900˚C for 1.5 hours for SOG and SOQ TFTs.

- Active island patterning
- Gate dielectric growth or deposition
- Gate poly-Si deposition at 620˚C
- Gate patterning
- Self-aligned S/D implantation
- Insulation layer deposition
- Dopant activation
- Contact hole opening and metallization

Figure 4. The device fabrication flow of SOG and SOQ TFTs.

4. Device Characterization

4.1 SOG TFTs

Measured drain current (I_d)-gate voltage (V_g) transfer characteristics of SOG TFT with channel width (W):length (L) ratio of 9.2μm:9.4μm are shown in Figure 5 for drain voltage (V_d) of 0.1V and 3V. μ_{FE} is the field-effect mobility extracted at the points of maximum trans-conductance, S is the sub-threshold

swing and the subscripts "n" and "p" of the parameters refer to n- and p-type TFTs, respectively.

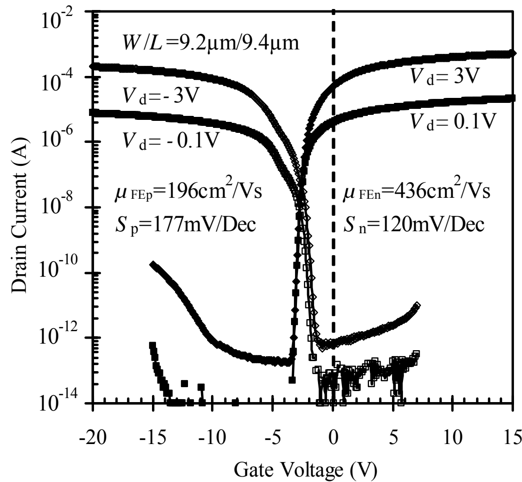

Figure 5. Transfer characteristics of n- and p-type SOG TFTs.

Shown in Figure 6 are the I_d-V_d output characteristics. At the same gate drive, I_d of an n-type TFT is 2 times greater than that of a p-type TFT. At high V_g and V_d, a negative differential resistance regime was observed for the n-type SOG TFT. This can be attributed to self-heating effect due to the significantly lower thermal conductivity of glass (~1W/mK) compared to Si (148W/mK).

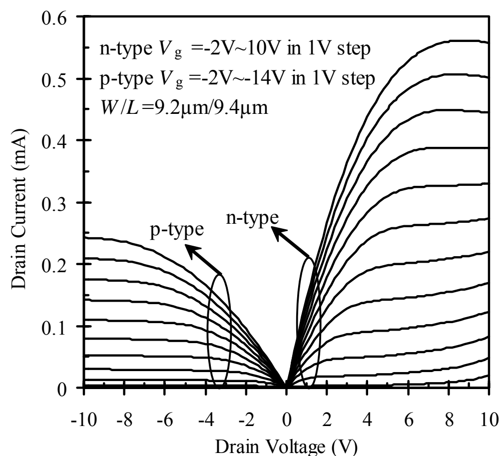

Figure 6. Output characteristics of n- and p-type SOG TFTs.

4.2 SOQ TFTs

Representative I_d-V_g curves for SOQ TFTs are plotted in Figure 7. As expected for TFTs built on fully insulating substrates, S values are close to the ideal room-temperature value of ~60mV/dec. The μ_{FEn} compares favorably to an electron μ_{FE} of 720cm^2/Vs for a TFT built on SOQ prepared using the bonding and etch-back technique [5]. The most likely reason for the higher electron μ_{FE} is the different technique of layer transfer adopted in the present work.

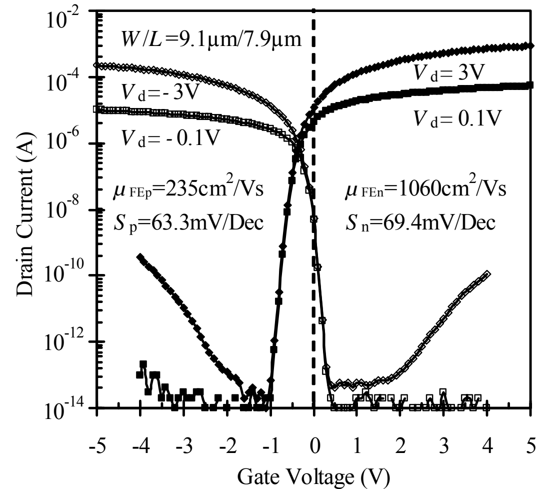

Figure 7. Transfer characteristics of n- and p-type SOQ TFTs.

Shown in Figure 8 are the I_d-V_d output characteristics. At the same gate drive, I_d of an n-type TFT is greater than 3 times that of a p-type TFT. At high V_g and V_d, self-heating effect was also observed for n-type device. It can be reduced by using pulsed V_d measurement.

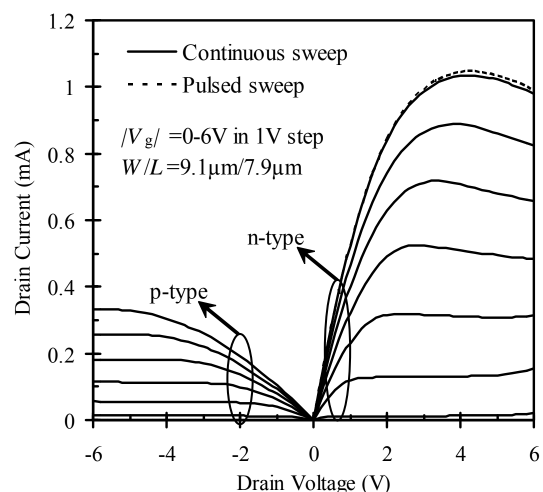

Figure 8. Output characteristics of n- and p-type SOQ TFTs. Pulsed V_d measurement was done with a pulse width of 0.5ms and a period of 1s.

4.3 Comparison between the SOG and SOQ TFTs

The major process/device difference between the SOG and SOQ TFTs are listed in Table I for reference.

Table I: Process/device parameters.

	Gate dielectric	Dopant activation	Highest temperature
SOG	~86nm (LTO)	550˚C, 8hrs	620˚C
SOQ	~28nm (Thermal oxide)	900˚C, 1.5hrs	1000˚C

The statistics of the measured electrical parameters are summarized and compared in Table II (a) and (b) for SOG and SOQ TFTs, respectively. R_s and R_c are the sheet and contact resistance of the source/drain regions. V_T is the linearly extrapolated threshold voltage. I_{Leak} is the minimum I_d. All of these parameters were extracted from the I_d-V_g transfer characteristics at $|V_d|$=0.1V.

Table II: Summary of electrical characteristics of (a) SOG and (b) SOQ TFTs.

(a)

	n-type		p-type	
	Average	Standard Deviation	Average	Standard Deviation
R_s (Ω)	103	30	1004	31
R_c (Ωcm^2)	3.2×10^{-6}	1.6×10^{-6}	2.5×10^{-6}	1.3×10^{-6}
μ_{FE} (cm^2/Vs)	416	17	191	10
V_T (V)	-2.26	0.36	-4.16	0.16
S (mV/Dec)	~130	9	~175	16
I_{Leak} (fA/μm)	<18	n/a	<23	n/a

(b)

	n-type		p-type	
	Average	Standard Deviation	Average	Standard Deviation
R_s (Ω)	102	8	198	12
R_c (Ωcm^2)	0.7×10^{-6}	3×10^{-8}	1.3×10^{-6}	4×10^{-8}
μ_{FE} (cm^2/Vs)	1060	49	220	12
V_T (V)	-0.17	0.05	-0.23	0.05
S (mV/Dec)	~73	3	~65	3
I_{Leak} (fA/μm)	<10	n/a	<6	n/a

The negative V_T measured for the n-type TFTs possibly resulted from a combination of positive charge in the gate dielectric and low channel doping concentration. The μ_{FE} of both n- and p-type SOG TFTs are smaller, while S and $|V_T|$ are larger than the corresponding values of SOQ TFTs. These can be attributed respectively to their inferior LTO/Si interface and relatively thicker gate dielectric. The SOQ TFTs shows more tightly distributed and smaller R_s and R_c. This can be attributed to the relatively more uniform and effective dopant activation resulting from the higher annealing temperature.

The vertical effective electric field (E_{Effn}) dependence of electron effective mobility (μ_{Effn}) for both SOG and SOQ n-type TFTs are plotted in Figure 9. For SOQ TFT, the low-field μ_{Effn} is 1072cm^2/Vs and about ~35% higher than that extracted from reported universal μ_{Eff} curve [12], which is also plotted in Figure 9 for reference.

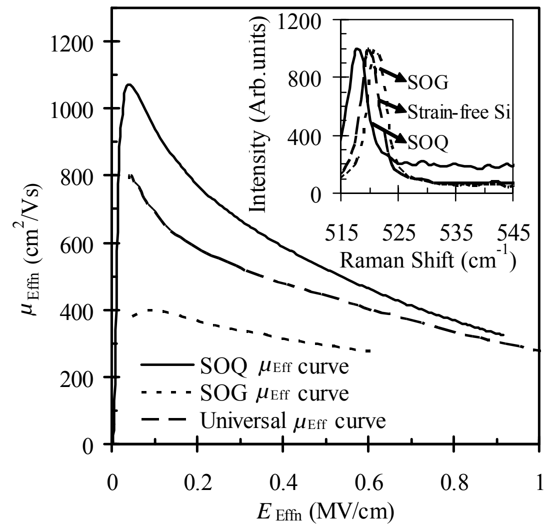

Figure 9. Dependence of μ_{Effn} on E_{Effn}. Shown in the Inset is the normalized micro-Raman spectrograms of SOG, SOQ and strain-free p-type bulk Si with a similar doping concentration of 10^{15}/cm^3.

With increasing E_{Effn}, μ_{Effn} decreases faster than the trend exhibited by the corresponding universal mobility curve. One likely reason is enhanced interfacial scattering due to the relatively rougher surface of the SOQ [13]. For SOG TFT, the low-field μ_{Effn} is ~400cm^2/Vs and is about 50% of that extracted from universal μ_{Eff} curve. The smaller μ_{Effn} of SOG TFT can be partly attributed to inferior LTO/Si interface.

Raman spectroscopy was performed after device fabrication. Shown in the Inset of Figure 9 are the Raman spectrograms of a strain-free p-type bulk Si and in the channel regions of SOG and SOQ TFTs. The peaks of the Raman shift increase in the order of SOQ (518cm^{-1}), stress-free Si (520cm^{-1}) and SOG (521cm^{-1}). This is consistent with compressive (~0.12%) and tensile (~0.24%) strain in SOG and SOQ [14], respectively. The μ_{Effn} enhancement of SOQ TFT is believed to be caused by the tensile strain, possibly originating from the significant difference between the CTEs of Si and quartz. The μ_{Effn} enhancement ratio is consistent with that reported previously [15]. The compressive strain, possibly caused glass shrinkage during the extended annealing, should also contribute partly to the reduction in μ_{Effn} of an SOG TFT.

5. Conclusion

Single-crystalline silicon on glass and fused-quartz substrates was prepared using wafer bonding and hydrogen-induced layer transfer. Thin-film transistors were subsequently fabricated on the resulting transferred silicon films and characterized. The high temperature processed devices on quartz exhibit superior device performance compared to low-temperature processed devices on glass. Compressive and tensile strain was respectively found in thin-film silicon on glass and on quartz. Enhanced effective electron mobility was found in the thin-film transistors built on the latter, consistent with the tensile strain.

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References

[1] X. Shi, K. Henttinen, T. Suni, I.Suni, S. S. Lau and M. Wong, IEEE Electron Device Letters, 24, 574(2003).

[2] D. N. Kouvatsos, G. T. Sarcona, D. Tsoukalas, M. K. Hatalis, D. Goustouridis, J. Stoemenos, AMLCDs, 125(1995).

[3] F. Plais, O. Huet, P. Legagneux, D. Pribat, A.J. Auberton-Herve, T. Barge, SOI Conference, 170(1995).

[4] T. Abe, K. Sunagawa, A. Uchiyama, K. Yoshizawa and Y. Nakazato, Japanese Journal of Applied Physics, Part 1, 32, 334(1993).

[5] K. R. Sarma and S. T. Liu, SOI Conference, 117(1994).

[6] Q.-Y. Tong, U. Gösele, T. Martini and M. Reiche, Sensors and Actuators A, 48, 117(1995).

[7] Q.-Y. Tong, T.-H. Lee, L.-J. Huang, Y.-L. Chao and U. Gösele, SOI Conference, 126(1997).

[8] Q.-Y. Tong, R. Scholz, U. Gösele, T.-H. Lee, L.-J. Huang, Y.-L. Chao and T. Y. Tan, App. Phys. Letters, 72, 49(1998).

[9] F. Brunier, O. Rayssac, I. Cayrefourcq, H. Oka, T. Sato, F. Fournel and C. Lagahe, SOI Conference, 59(2003).

[10] K. Henttinen, T. Suni, A. Nurmela, I. Suni, S.S. Lau, T. Höchbauer, M. Nastasi and V.-M. Airaksinen, Nuclear Instruments and Methods in Physics Research B, 190, 761(2002).

[11] F. Lu, J. Bickford, C. Novotny, P. K. L. Yu, S. S. Lau, K. Henttinen, T. Suni and I. Suni, Journal of Vacuum Science & Technology B, 22, 2691(2004).

[12] S. Takagi, A. Toriumi, M. Iwase and H. Tango, IEEE Trans. on Electron Devices, 41, 2357(1994).

[13] G. Mazzoni, A. L. Lacaita, L. M. Perron, A. Pirovano, IEEE Trans. on Electron Devices, 46, 1423(1999).

[14] J. C. Tsang, P. M. Mooney, F. Dacol and J. O. Chu, Journal of Applied Physics, 75, 8098(1994).

[15] J. L. Hoyt, H. M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E. A. Fitzgerald and D. A. Antoniadis, Electron Devices Meeting, 23(2002).