A 2.4-in QVGA p-Si LTPS AMLCD for Mobile Application

Yu-Cheng Chen
Central Research Institute, Chunghwa Picture Tubes, LTD., Taoyuan,Taiwan
Tai-Ming Lin, Tien-Chu Hsu
Central Research Institute, Chunghwa Picture Tubes, LTD., Taoyuan,Taiwan

Abstract
A 262K-color QVGA LTPS AMLCD was developed. This panel has integrated gate driver and data multi-plexer (1:3) by p_Si LTPS TFT process. The commercialized driver IC was adopted to implement this display. Fine image quality, low power consumption and cost-efficiency feature make the panel be suitable for mobile application.

1. Introduction
The demand has been growing recently in the mobile industry such as DSC (Digital Still Camera), PMP (Portable Media Player), mobile phone etc. All of these applications are possible with the low cost, fine image quality, and low power consumption display. Under 2.5-inch size, the a-Si AMLCD still dominates the QCIF and QCIF+ market by its advantage of low cost. When resolution increases to QVGA, the a-si AMLCD is unable to satisfy the requirement because of lower aperture ratio debasing image quality and raising power consumption of backlight.

The CMOS LTPS AMLCD has been developed for several years and the driver, power and control circuit can be integrated on the glass to reduce external electronic devices [1] [2] [3]. This technology has good performance on image quality and power consumption, but 7 to 9 mask processes are more than the conventional 5 mask processes of a-Si AMLCD result in reducing the yield rate and increasing cost of LCD manufacturers [4].

The LTPS PMOS AMLCD can be accomplished by 5 to 7 masks as a-Si AMLCD compared with LTPS CMOS AMLCD for cost-down issue. It also integrates partial driver circuit to provide the features of high resolution and low power consumption for future advanced mobile display.

For the reason above, we develop the 2.4” PMOS LTPS AMLCD that can provide both high performance and superior productivity to meet market requirement.

2. p-Si Characteristics
On the basis of our process, we have fabricated the p-Si TFT with proper characteristics to achieve integration of the circuits. The device ought to possess rapid mobility to meet operating frequency at ~MHZ range and provide low threshold voltage to reduce voltage swing and power consumption.

Fig1.shows the transfer curves of p-Si TFT. The channel width and length of the device are 8μm and 8μm respectively. V_{th} and μ_h are –1.7V and 90cm^2/Vs. Although the characteristics are not great, it is enough for our requirement.

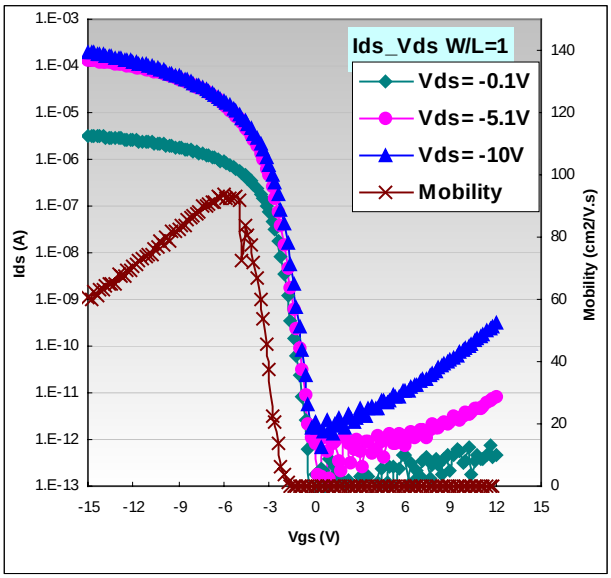

Fig.1 Characteristics of p-Si TFT

3. Implement of p-Si LTPS AMLCD

3.1 LCD Module Structure
Fig.2 shows the block diagram of 2.4” PMOS LTPS AMLCD. It consists of gate driver as well as 1:3 multi-plexer integrated on the glass substrate and the commercialized COG driver IC. The COG chip can apply the signal that we need and powerful function that PMOS structure is difficult to achieve. In fact, the commercialized COG driver IC can be obtained easily from IC maker. If volume grows up, the price of COG IC will drop rapidly.

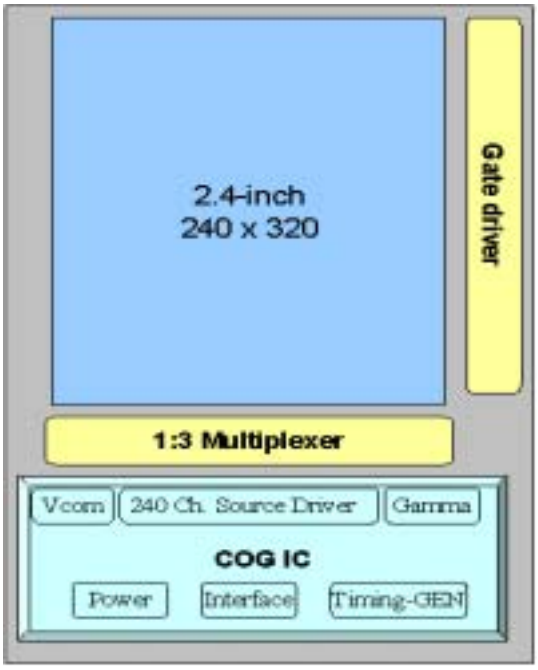

Fig.2 Block Diagram of 2.4" QVGA p-Si AMLCD

3.2 AC Vcom Driving Scheme

Because the Cst is formed by metal-insulator-semiconductor structure, Cst has to keep maximum depletion region so that Cst will not vary with the potential on the pixel electrode. To keep Cst with maximum depletion region, common electrode need to apply proper negative voltage. When AC Vcom signal is applied from COG Chip, the common electrode will be applied the signal shown in Fig.3 to retain correct charge in Cst.

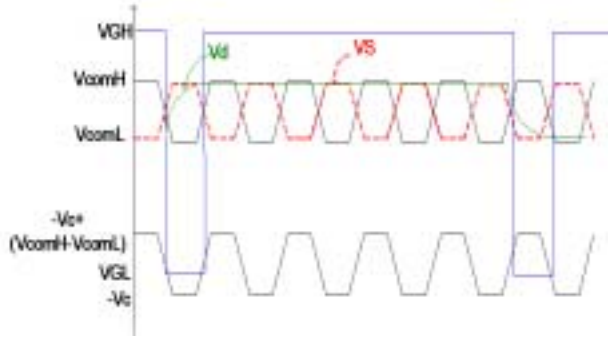

Fig.3 AC Vcom Driving Waveform

Since the COG Chip provides AC Vcom signal, the voltage swing of source and gate signal can be reduce to lower the power consumption. It should also be added that this p-Si panel with aperture ratio about 65% is higher than a-si panel with that about 50%. Higher aperture can offer higher light throughput to save the power of backlight.

3.3 Gate driver

In this panel, 1:3 multiplexer and gate driver is integrated using PMOS LTPS technology. The 1:3 multiplexer is simply implemented by PMOS switches and fast enough for data signal selection.

The gate driver block diagram is shown in Fig.4.It composed of a series of S/R latch combining with buffer. This structure separates output signal and shifting signal into different path, which can ensure gate driver driving capacity and shifting function.

Fig.5 is the timing diagram for gate driver. The Sin signal is the start pulse of shift register and 2-phase clock signal is used to operate shift registers. The swing level of clock signal decides the gate driver output signal applied to gate electrode of panel. Because of adopting AC Vcom driving scheme and the outstanding characteristics of PMOS TFT, the swing level of clock can be diminished to the peak to peak voltage of 14V for driving panel TFT and therefore reduce the power consumption.

Fig.6 shows CLK input signal and the last stage of gate driver output waveform at the CLK frequency of ~8kHz.The waveform of last stage with less delay can be accepted.

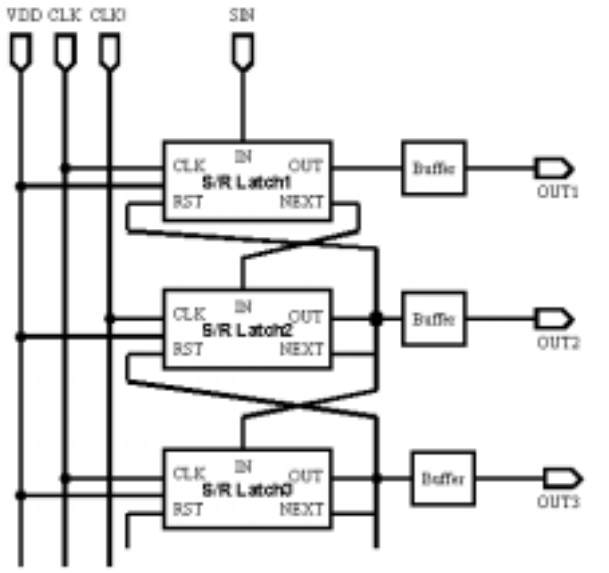

Fig.4 The Block Diagram of the Gate Driver

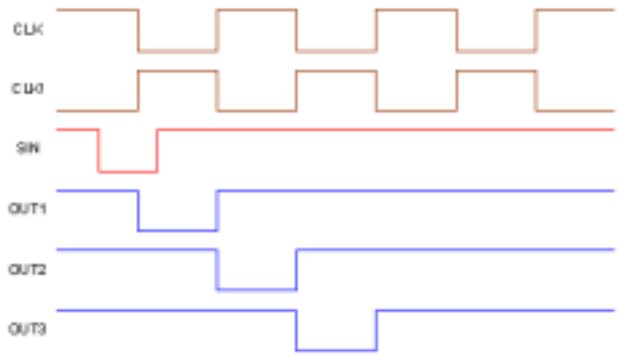

Fig.5 The Timing Diagram of the Gate Driver

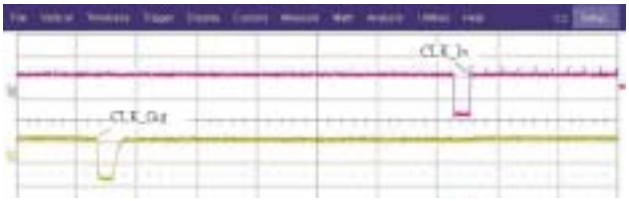

Fig.6 Output Waveform of the Gate Driver

4 Performance of LCD module

Table1 shows the specification of the display, which has been fabricated in PMOS LTPS. The photograph of fabricated modules with a pretty image is shown in Fig 6..The transmittance of the panel is more than 7%. The power consumption of LCD module excluding that of backlight is 18mW at the frame rate of 60Hz. Furthermore, the integration of gate driver and the 1:3 multiplexer can reduce bezel size for mobile application.

5 Summary

We have developed a 2.4-in p-Si LTPS AMLCD. The panel integrated gate and data driver circuit has been implemented by using PMOS circuit. The display is skillfully with the commercialized driver IC to achieve high performance. Furthermore, the advantage of reducing production cost due to PMOS only process can compete with a-Si and CMOS LTPS upon mobile application market.

Table 1. Panel Specification

Display Area(in mm)	36.576(W) x 48.768(H)
View Area(in mm)	39.6(W) x 51.8(H)
Number of Pixels	240(W) x 320(H)
Pixel Pitch(in mm)	0.051x0.153
Color Pixel Arrangement	RGB vertical strip
Display Mode	normally white
Number of Colors	262K
Brightness(cd/m^2)	220nit
Contrast Ratio	200:1
Response Tims(Tr+Tf)	30ms
Viewing Angle	45/-45 degree(Horizontal)
(BL ON ,CR> 10)	50/-30 degree(Vertical)
NTSC Ratio	45%
Luminance Uniformity	80% in white color
Input Signals	RGB I/F line inversion
outline dimension(in mm)	45.8(W) x 62.1(H) x 3.3(D)
Viewing Direction	12 o'clock
BL unit	LED
weight(g)	15g

Fig.7 Photography of 2.4" QVGA p-Si LTPS AMLCD

6 Reference

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