Microcrystalline Si TFTs with Low Off-Current and High Reliability

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Abstract
Microcrystalline Si (µc-Si) TFTs were fabricated using a conventional bottom gate amorphous Si (a-Si) process. A unique µc-Si deposition technique and TFT architecture was proposed to enhance the reliability of the TFTs. This three-mask TFT fabrication process is comparable with existing a-Si TFT procesess. In order to suppress nucleation at the bottom interface of Si, before deposition of the µc-Si an N_2 plasma passivation was conducted. A typical transfer characteristic of the TFTs shows a low off-current with a value of less than 1 pA and a sub-threshold slop of 0.7 V/dec. The DC stress was applied to verify the use of µc-Si TFTs for AMOLED displays. After 10,000 s of application of the stress, the off-current was even lowered and sub-threshold slope variation was less than 5%. For AMOLED displays, OLED pixel simulation was performed. A pixel current of 13 µA was achieved with V_{data} of 10 V. After the simulation, a linear equation for the pixel current was suggested.

1. Introduction
Recently, amorphous Si (a-Si) based thin-film transistors (TFTs) used as a backplane for active matrix organic light emitting diodes (AMOLED) have attracted a lot of attention [1,2]. However, the performance of a-Si TFTs still needs to be improved in such area as off-current, mobility, and reliability. The fact that a-Si TFTs can make only n-channel TFTs is another drawback for integrated AMOLED displays in the future. For AMOLED displays, threshold voltage degradation of a-Si TFTs by gate voltage bias is one of the most serious problems as well [3]. Polycrystalline Si (poly-Si) based TFTs showed higher TFT performance, but at the present time, they require more process steps and show non-uniformity over large areas. [4].

Microcrystalline Si (µc-Si), on the other hand, has the potential to be employed in AMOLED displays in the future. The same and well-established bottom-gate a-Si TFT fabrication process and equipment can be used in the existing LCD manufacturing facilities. The TFT performance could be greatly enhanced compared with a-Si TFTs (for example, mobility more than 100 cm^2/Vs) [5]. However, a typical µc-Si TFT characteristic shows relatively high on-current and high mobility only when the off-current is high. Threshold voltage instability after electrical stress is also a drawback of the some of the conventional µc-Si TFTs.

In this paper, we report highly reliable bottom-gate µc-Si TFTs. In order to raise the probability of being implemented in products such as AMOLED displays, an existing a-Si TFT fabrication process was adopted. We can even use the same photo masks for TFT fabrication as for a-Si TFTs. Our research is focused on the aspect of having high-performance and stable TFTs using µc-Si as opposed to improving the mobility of the TFTs.

2. Experimental
Microcrystalline TFTs were fabricated using a conventional bottom-gate process. 200-nm-thick Cr was used as a gate metal on glass substrates. After deposition of 350-nm-thick SiN_x as a gate insulator, an N_2 plasma passivation was conducted for a few minutes at 200 ℃. We expected that this plasma treatment would reduce the number of random nucleation sites at the µc-Si and SiN_x interface [6].

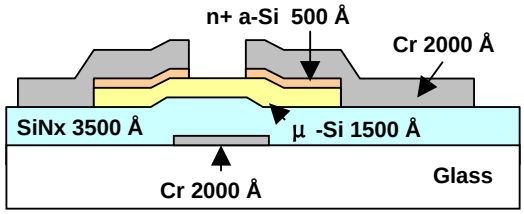

Figure 1. Schematic cross-section of bottom-gate µc-Si TFT

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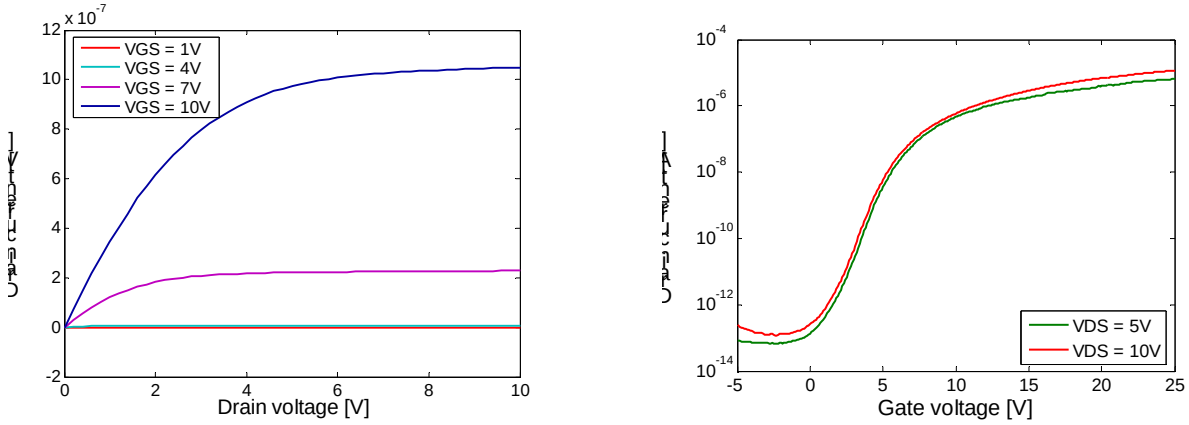

(a) (b)

Figure 2. Typical output (a), and transfer (b) characteristics of µc-Si TFTs (W/L=200/10 µm)

After the plasma treatment, 250-nm-thick µc-Si and 50-nm-thick n^+-Si were consecutively deposited using RF-PECVD to avoid unnecessary oxidation of the active layer. For the µc-Si, two different deposition techniques were used. First, a standard hydrogen dilution method was used: a silane–hydrogen gas mixture at 250 ℃ and pressure between 2000 and 2500 mTorr. For this method, the $SiH_4/(SiH_4+H_2)$ flow ratio and the power density are critical to the quality of µc-Si. Second, SiF_4 gas mixed with Ar and H_2 gases was used. Deposition rate of µc-Si ranged from 1~10 Å/s, depending on the deposition conditions. The deposition rate, as well as the quality of the µc-Si thin film, can also be controlled by the H_2 dilution rate and the sample-to-electrode distance. The details of fabrication of µc-Si thin films can be found elsewhere [6]. Phosphine was used as a dopant source during n^+ layer deposition. After defining n^+-Si and µc-Si using a second photo mask, 200-nm-thick Cr was deposited as a source and drain layer. After fabrication of the TFTs, a short- time thermal anneal was performed. The properties of intrinsic and n^+-doped Si layers were tested before TFT fabrication. For this purpose, single-layer depositions were made using the same conditions as for TFT fabrication. Film properties were characterized by Raman scattering and spectroscopic ellipsometry (SE) measurements. Some samples had additional process steps, such as SiN_x passivation, via, metal, ITO, and OLED deposition for the measurement of invertors, ring-oscillators, and OLED pixel measurements.

Figure 1 demonstrates the cross-section of the bottom-gate µc-Si TFT structure. The stress test was performed using 20-V gate bias at room temperature for 10,000 s.

3. Results and Discussion

Figure 2 shows typical output and transfer characteristics of the µc-Si TFTs. As one can see from Fig.2(a), as the gate voltage increases, the TFT shows stable characteristics without current crowding or the kink current effect. The on-current, off-current, and sub-threshold slope were $1.2\text{x}10^{-5}$, $1.2\text{x}10^{-13}$, and 0.7 V/dec, respectively. For pixel TFTs in AMOLEDs, a low off-current and good uniformity are the most critical requirements [1–5].

Without complicated lightly doped drain (LDD) or dual-gate structures, an off-current on the order of 10^{-13} A was achieved. This is due to the fact that our method to make µc-Si is suitable for this specific bottom-gate TFT structure.

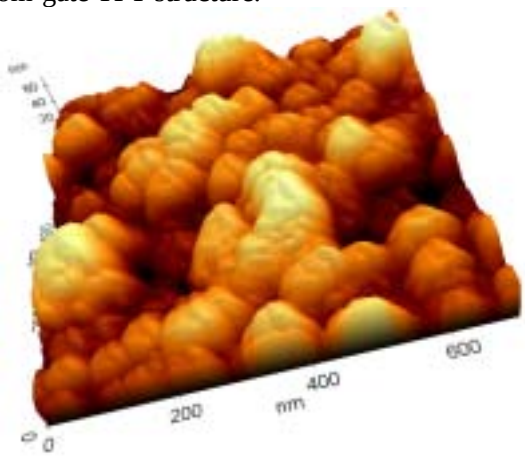

Figure 3 3D AFM image of a µc-Si thin film.

Table 1. Properties of µc-Si films from SE spectra

µc-Si layer	Thickness, Å	F_c, %	F_a, %	F_v, %
bulk	2240	94	6	-
subsurface	452	97	-	3
roughness	61	63	-	37

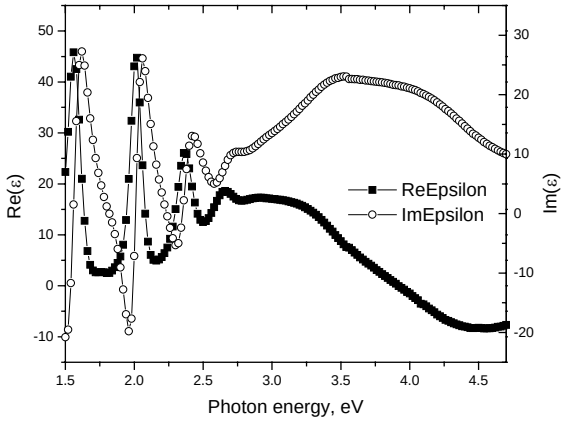

Figure 4. Calculated spectral dependence of the real (Reε) and imaginary parts (Imε) of the pseudo-dielectric function for a representative µc-Si thin film.

The low and stable off-current can be attributed to the stable Si/SiN_x interface. In addition to the good interface properties, because the substrate temperature is quite low, the level of oxygen impurities must be low. As mentioned in the previous section, the N_2 plasma treatment can be favorable effect on the grain size of µc-Si [6]. For better µc-Si thin films, we tried to increase the movement of Si at the surface; to etch the unstable Si; and to control the H movement, to optimize the effect of *chemical annealing* on crystallization. If the growth rate was too fast, we might have obtained an amorphous phase at the bottom of the µc-Si films.

Figure 3 shows 3-D AFM images of µc-Si. We noticed that the grain size ranged from 80 to 120 nm, and the surface roughness ranged from 6 to 10 nm.

According to the SE results in Fig.4, the µc-Si had crystal fraction of more than 90%. Spectroscopic Ellipsometry measurements were performed in the range 1.5~4.7 eV. The spectral dependence of the real (Reε) and imaginary parts (Imε) of the pseudo-dielectric function calculated from I_s and I_c are shown in Fig.4. The SE data were fitted using the Bruggman Effective Medium Approximation (BEMA) method to get the structure of the films in terms of composition, roughness, and thickness [7]. In the BEMA model, the µc-Si layer was described as a mixture of a-Si, poly-Si, and voids. In the optical model used to fit the experimental data, we considered the film as a three-layer structure consisting of a bulk layer, a subsurface layer, and a thin layer representing the surface roughness. The thickness and composition of all layers are listed in Table 1.

Figure 5 shows TFT characteristics during and after the electrical stress. The stress condition was V_{gs}=25 V, V_{ds}=10 V, applied for 10000 s. It is interesting to note that the off-current is reduced with increasing duration of application of stress. On the other hand, the on-current level is not much reduced. Presumably, this is due to the fact that the active channel region has a high crystal fraction ratio. Typically, high-reliability TFTs are associated with poly-Si or single-crystal Si TFTs with the LDD, dual- gate, or offset structure. For these specific µc-Si TFTs stable TFTs were fabricated without using complicated additional processes like LDD,.

Figure 6 also shows the TFT characteristics during and after DC stress. Fig. 6 shows the variation of sub-threshold slope (V/dec) and the variation of mobility (cm^2/Vs). The initial value of the slope was approximately 0.7 V/dec. Even after 10000 s, this value stays more or less the same. The mobility varies from 1 to 10 cm^2/Vs. The initial variation was less than 5% and after 10,000 s of application of stress, it reaches approximately 10% of the mobility.

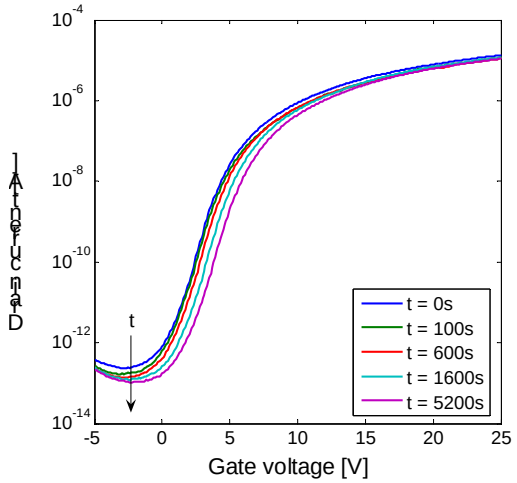

Figure 5. Transfer characteristics during and after DC stress. V_{ds} is 10 V. The size of the TFT was 200/10 µm (W/L)

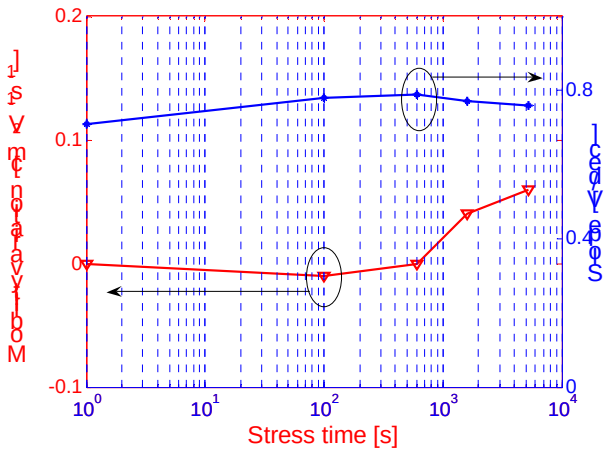

Figure 6. Reliability of µc-Si TFTs: sub-threshold slope and mobility variation during the DC stress.

Figure 7(a) shows the schematic pixel circuit for AMOLEDs and Fig. 7(b) shows the simulation and fitting results of the pixel current. Implementing the experimental TFT results on an AIM-SPICE simulation resulted in pixel currents of 10~13 µA with V_{DD} ranging between 8~10 V. The basic parameters for the simulation were as follows: V_{CC} =15 V, V_{select} =15 V, pulse time=0.2 ms, capacitance=100 pF. Based on the simulation results, we have deduced the following equation

$$I_{OLED} = A(V_{data} - V_{th})^{\sqrt{3}}$$

where, I_{OLED} is the current level of an AMOLED pixel.

4 Conclusion

Without changing the existing a-Si TFT fabrication process, and using the same masks as for a-Si TFT fabrication, we have developed a unique µc-Si TFT with low off-current and high stability. The maximum process temperature was 250 ℃. Due to the high crystallinity at the bottom interface and stable Si/SiN_x interface, the off-current of the TFTs stays even after application of DC stress for extended period of time. After removal of the stress, the residual TFT degradation was almost negligible. Based on the experimental TFT results, we have simulated the current level of OLED pixel as 13 µA.

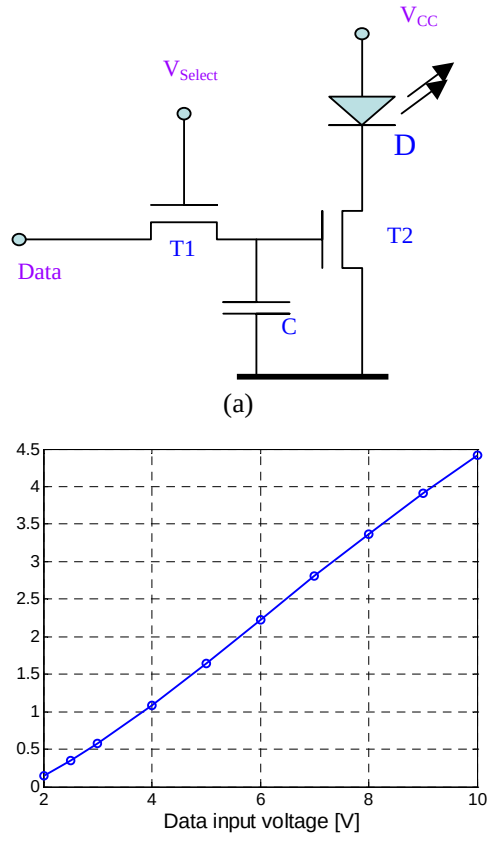

Figure 7. (a) Schematic circuit diagram for an AMOLED pixel, (b) Current simulation results: TFT size is 100/5 µm (W/L).

5. Acknowledgements

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6. References

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