Integrated Gate Driver Circuit Using a-Si TFT with AC-Driven Dual Pull-down Structure

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Abstract

Highly stable gate driver circuit using a-Si TFT has been developed. The circuit has dual-pull down structure, in which bias stress to the TFTs is relieved by alternating applied voltage. The circuit has been successfully integrated in 4-in. QVGA and 14-in. XGA TFT-LCD with a normal a-Si process, which are stable for over 2,000 hours at 60°C. The enhancement of stability of the circuit is attributed to retarded degradation of pull-down TFTs by AC driving.

1. Introduction

Integrating driver circuits on the glass is important in the LCD technology, because cost can be reduced by eliminating the driver IC's and relating processes. It has long been regarded that poly-Si technology is the most probable way for this purpose. Poly-Si TFT has superior device performance to a-Si TFT. It seems that embodiment of driver circuits and some control parts on glass are now technologically attainable and the integration level will be even higher. However, most active matrix LCD manufacturers are based on a-Si technology, additional cost must be taken into account to adopt the poly-Si technology.

On the other hand, depositing drive circuits using a-Si TFT has been attracting interest [1,2,4,8] since it has advantage of using the same process with TFTs in pixel arrays. There are two things to consider in designing practical circuits using a-Si TFT.

First, a-Si TFT has low mobility. It is about $0.5cm^2/Vs$, an order of a hundredth of that of poly-Si TFT. The size of TFTs in circuits must be increased up to more than thousands of microns for driving gate lines which has about a thousand times as large capacitance as pixels. Large a-Si TFTs are yet to be well characterized. Then, instability of a-Si TFT is a far more serious problem. When a TFT is biased for a long time, the electrical properties change. Threshold voltages of a-Si TFTs in a circuit increase with time while the circuit is working. The circuit finally ceases proper operation. Insufficient life time of circuits has been the critical barrier to prevent a-Si TFT drivers from being practical technology. Efforts have been made to make more stable TFT by changing process and/or modifying device structures. In this case, no loss of productivity and yield in the manufacturing process must be guaranteed.

In this paper, we would like to present a practical a-Si gate driver circuit which can be fabricated with present a-Si technology for mass production. Results and discussion of enhanced stability of 4-in. QVGA and 14-in. XGA gate driver integrated panel (GIP) will be given.

2. a-Si Gate Driver Circuit

2.1 Conventional a-Si Gate Driver

Figure 1 is the block diagram of a unit of a conventional gate driver using a-Si TFT. An a-Si gate driver ordinarily works as a shift register. Each unit

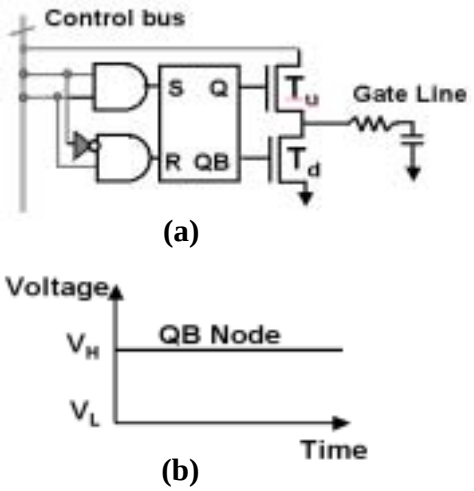

Figure 1. (a) Schematic block diagram of a conventional gate driver unit and (b) voltage of QB node in the circuit. Nearly DC gate bias is applied to QB node

gives high voltage output during one horizontal time in one frame time, keeping the gate lines connected to it at high voltage state while pixels controlled by the gate line are charged to certain data levels. After the pixels are charged, the gate line has to become the low voltage state for keeping the stored charges in the pixels until next scan time. So, for TFT-LCDs, the gate lines are maintained at low voltage almost all the time during operation. To make low voltage of gate lines stable, the pull-down transistor (Td) is kept at a conducting state. It is required that the QB node in the gate driver be biased high nearly constantly, which causes severe threshold voltage shift of TFTs whose gate electrodes are connected to the QB nodes.

2.2 a-Si TFT Instability

The instability of a-Si TFT due to bias stress has been investigated by many researchers [5,9]. Threshold voltage of a-Si TFT changes when it is biased for a long time.

Figure 2 is the plot of change in transfer curves of an a-Si TFT subject to bias stress. The TFT was made under the same process that circuits are made. Measurement was done at 60°C with stress bias condition Vgs=30V and Vds~0V, under which TFT works in linear region. As can be seen in the figure, the curve is shifted parallel. It follows that mobility and subthreshold slope don't change much when Vth shift amounts up to over 10V. Charge trapping may account for the parallel shift of the curve under the stress condition [6, 9].

2.3 Instability of a-Si Gate Driver

Nearly DC bias is applied to the pull-down TFTs in normal gate driver circuits. So the TFTs become degraded rapidly during working. In some circuits, the pull-down TFT is designed to be turned-off to circumvent this situation [2]. We understand that the QB nodes should sustain a certain level of voltage for proper operation of the circuits. This voltage was found to increase as the diver circuit is working. This can be used to describe a degree of degradation of a driver circuit. We introduced the "clamping voltage" of a circuit, which may be considered as the "age of a circuit"[7]. The clamping voltage increases as a circuit gets degraded owing to bias stress for long time working. The circuit finally becomes mal-functioning when the clamping voltage exceeds a preset limit, which may be a voltage applied to the circuit. The failure of circuit operation due to bias stress may be thought to be from the noise voltage generation through coupling and its amplification during propagation. Correlation between the clamping voltage and Vth of a TFT is seen clearly in Figure 3. The symbols (square and circle) show change of Vth of a TFT under DC bias. The data of clamping voltage against time can be fitted with *Vth + constant*. So, increases in the clamping voltage can be explained by the Vth shift of pull-down TFTs. We will present more detailed analysis elsewhere.

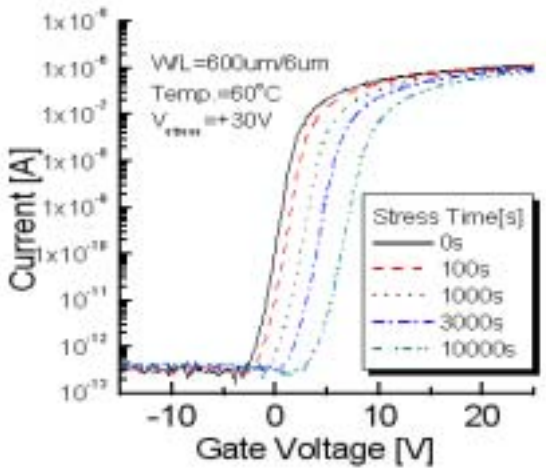

Figure 2. The transfer curves shift to the positive direction owing to positive bias stress in linear region, which results in increases of Vth.

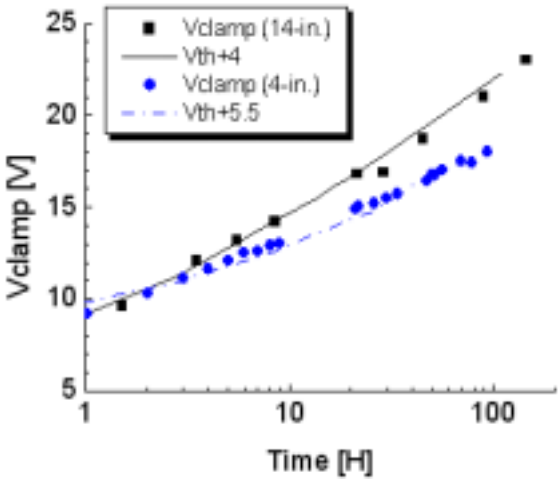

Figure 3. Vth shift of TFTs and clamping voltages of a circuit. Stress bias is 25V (solid line) and 20V (dash dot). Vth shift accounts for the increase in clamping voltages

Consequently the failure of a conventional gate driver circuit is from inability of maintaining QB nodes at voltages to make the pull-down TFTs have sufficient conductance.

3. a-Si Gate Driver with AC Driven Dual Pull-down Structure

3.1 Basic Operation

Figure 4 is the block diagram of the new gate driver circuit. Differently from the conventional circuits, it consists of a pair of pull-down transistors.

The two pull-down transistors take charge of keeping a gate line in low state alternately. In this circuit, voltages of the two nodes QB1 and QB2 which are respective gate electrodes of the two pull-down transistors change switchedly. In the dual pull-down structure circuit, the gate voltage of the QB-connected TFTs can be viewed as pulse-shaped with 50% duty (Figure 4(b)). The bias stress is expected to be stopped when a TFT is turned off – so it can be called AC bias stress.

3.2 Retarded Degradation of Circuits

Stability of our new driver circuit was verified for both 4-in. QVGA and 14.1-in. XGA panel. Figure 5 is a plot of clamping voltages vs. time when the circuit

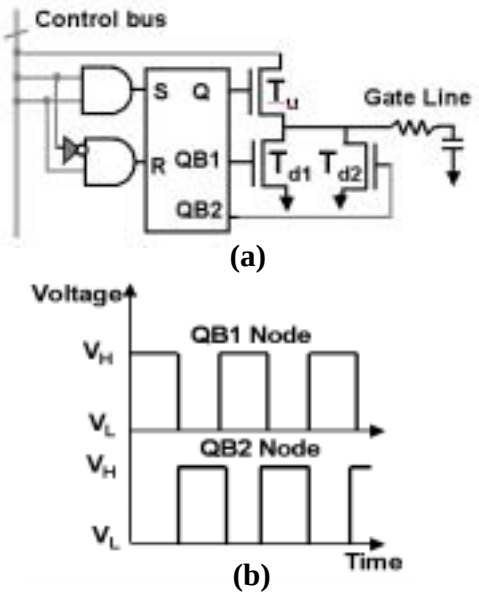

Figure 4. (a) Schematic block diagram of gate driver circuit with the dual pull-down TFTs structure and (b) timing diagram of two QB-nodes of gate driver

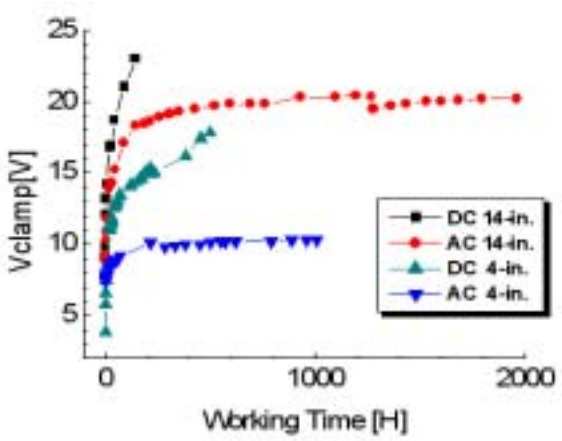

Figure 5. Increase in clamping voltage of AC driven circuits is retarded while DC biased conventional circuits reach spec limits fast.

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is working at 60°C. It is seen that degradation of our new circuit is dramatically suppressed. While panels with DC-driven circuits have finite working times around a few hundred hours, the panels with new AC-driven circuits show no failure within our measurement time. The slower increase of clamping voltage even seems to be saturated in linear time scale to a spec-in level, which is expected to guarantee much longer life time. The apparent retardation of degradation of circuits is caused by relieved stress to AC-driven pull-down TFTs.

We measured Vth shift of a-Si TFTs under pulse bias stress [10]. The efficiency of AC stress bias can be calculated as the relative shift of Vth compared to that under DC bias, with the condition that the total amount of stress time was equal. Likewise, the efficiency in AC-driven circuits can be also estimated as the relative shift of clamping voltage in comparison with DC circuits. In figure 5 is shown the plot of efficiency of stress to circuits with time. Marked with a star is from the previous result of TFT [7,10], which corresponds to early stage of degradation. The x-axis represents the total stress time, which is the sum of time when bias of QB node is high and equals the total working time multiplied by the duty ratio. The efficiency is below 1 and decreasing with time: even though the amount of accumulated stress time is the same, the bias in the form of pulse is less effective for degrading a-Si TFTs [3]. It is attributable to relaxation of degraded states while the bias is stopped, which is known as metastability of a-Si TFT. The efficiency of

stress bias at AC operation is expected to become

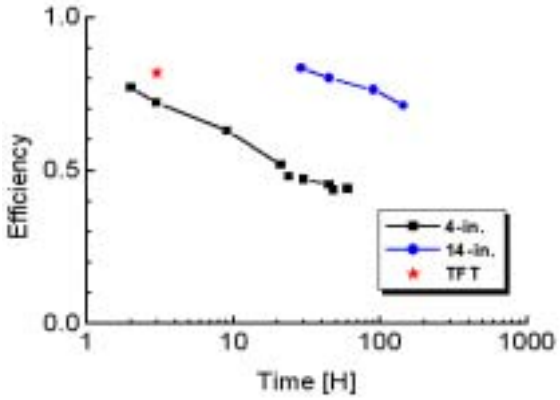

Figure 6. Efficiency of bias stress in gate driver circuits measured as relative clamping voltage shift of an AC circuit with respect to a DC circuit. The star symbol stands for efficiency for a TFT.

smaller as degradation goes on, owing to the stronger tendency of relaxation when a TFT is deviated farther from it's equilibrium state [5].

3.3 Gate Driver Integrated Panels

Fabrication of the new a-Si gate driver can be done without any difficulty. We made gate driver integrated panel (GIP) of 4-in. QVGA and 14.1-in. XGA with normal process [7,10]. The QVGA a-Si gate driver consisting of a 240 stages shift register was integrated in one side of a panel while 768 stages shift register for XGA was integrated on both sides in consideration of circuit area. They show very stable performance with good quality for more than 2000 hours at 60^{o}C.

4. Summary

We presented a novel gate driver using a-Si TFT having dual pull-down transistors which alternately work for maintaining gate lines at the low voltage state. The transistors are under AC bias, which results in much less degradation compared to those under DC bias stress in conventional circuits. The panels with the integrated gate driver have been successfully fabricated with good display quality, which shows extremely high stability at elevated temperature.

5. Acknowledgements

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6. References

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