Characteristics of a-Si:H TFTs with Silicon Oxide as Passivation Layer

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Abstract

The characteristics of a-Si:H TFTs with silicon oxide as passivation layer were reported. It was studied that the insulating characteristics and step coverage characteristics of low temperature silicon oxide before applying to a-Si:H TFT fabrications. With the optimum deposition conditions considering electrical and deposition characteristics, low temperature silicon oxide was applied to a-Si:H TFTs. The changes in characteristics of a-Si:H TFTs were analyzed after replacing silicon nitride passivation layer with low temperature silicon oxide layer. This low temperature silicon oxide can be adapted to high resolution a-Si:H TFT LCD panels.

1. Introduction

High-resolution displays with pixel densities larger than 300 ppi are developed today. The valued of a large display is obvious: it shows more information at one time so that the visualization is more complete and efficient [1]. In these days, large part of the high resolution displays are fabricated with poly-Si TFTs which are superior to a-Si:H TFTs in a viewpoint of TFT characteristics. But it is hard to adopt poly-Si TFT panel to large display module such as monitor because of its fabrication difficulty. One of the best solution to solve these problem is high resolution a-Si:H TFT panel with copper electrodes which are actively developed now [2].

When the resolution of the panel goes higher, some problems are emerged such as RC delay in the interconnect lines which could degrade the quality of display images. The copper electrode line will decrease the resistance of metal line due to its low resistivity. But for the resistance of the metal line, the capacitance of interdielectric layer also should be decreased to reduce the RC delay of input signals. In nowadays, silicon nitride layer with dielectric constant of ~7.5 is used for passivation layer in TFTs, which could make high RC delays. Although some organic thin films with low dielectric constant were used for passivation layer, its process cost are higher than the inorganic layer such as silicon nitride and silicon oxide.

We developed silicon oxide passivation layer for high-resolution panels with lowering RC delay. The characteristics of low temperature silicon oxide were optimized and the film was applied to a a-Si:H TFTs. The characteristics of TFTs were studied after adopting silicon oxide layer.

2. Experimental

2.1 Thin Film Deposition and Characterization

The deposition temperature of silicon oxide by PECVD was set to 300℃, which was lower than the deposition temperature of a-Si:H active layer, in order to prevent the degradation of active layer. For the electrical characterization of silicon oxide layer, we measured I-V characteristics with metal-insulator-metal (MIM) structure as shown in Figure 1. The length and width of the line shape was defined after WQUXGA panel design rule. The thickness of silicon oxide between the metal lines was set to 3000Å. For the I-V measurements, applied voltage was swept

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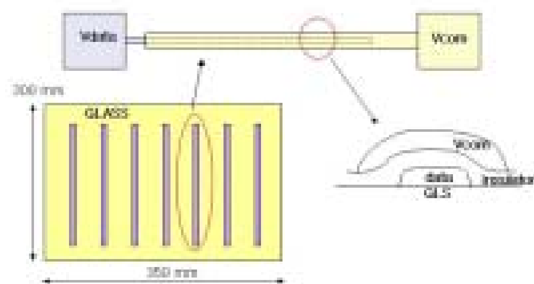

Figure 1. MIM structure for I-V measurements

from 0 to 200V and the leakage current was calculated considering the shape of metal line designs, its width and length.

2.2 TFT Fabrication and Characterization

Bottom gate type a-Si:H TFTs were fabricated by 5 Mask process to investigate the effect of silicon oxide passivation layer. Two types of TFTs were fabricated at the same time in order to investigate the effect of silicon oxide: TFTs with silicon nitride and TFTs with silicon oxide passivation layer.

3. Optimization of silicon oxide layer

For the deposition of silicon oxide by PECVD, SiH_4 and N_2O were used as a reaction gas. To find the optimum deposition conditions as passivation layer, RF power, chamber pressure and gas ratio were varied during silicon oxide deposition process. There are two main points that should be considered to adopt silicon oxide as a passivation layer in TFTs. The first is quality of silicon oxide, obviously. The second is its step coverage characteristics. When the step coverage characteristics of passivation layer are poor although its electrical quality is very good, there would be high leakage current and easy dielectric breakdown on passivation layer. One weak point in passivation layer on the long data line could be turn into the origin of leakage current, easily. Where the step coverage characteristics are poor, the thickness of the passivation layer on this weak point is thinner than normally deposited area so that dielectric breakdown could be happened. Figure 2 shows two I-V characteristics of silicon oxide with respect to its step coverage. In Figure 2 (a), although the amount of leakage current is high due to poor quality of silicon oxide, it does not show soft breakdown until electric field is larger than 5MV/cm.

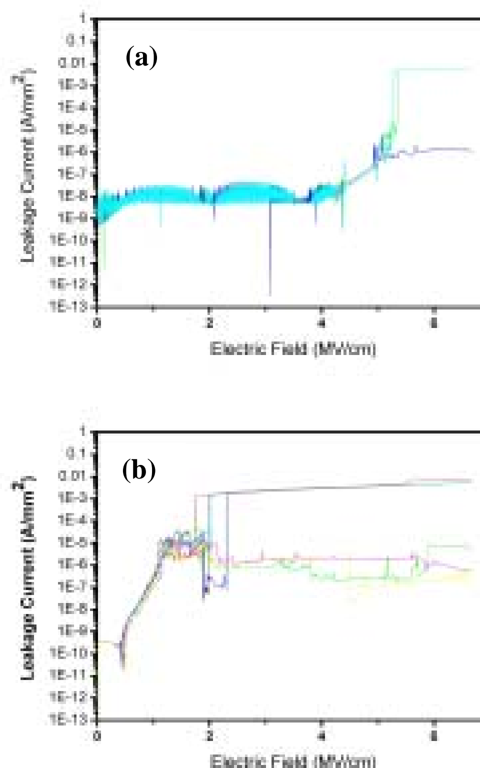

Figure 2. I-V characteristics of silicon oxide
(a) good step coverage
(b) poor step coverage

Meanwhile, Figure 2 (b) shows early soft breakdown point under 1MV/cm. For the layers in Figure 2 (b), the amount of leakage current is lower than that of Figure 2 (a) when the electric field on the passivation layer is low. This means that the quality of silicon oxide in Figure 2 (b) is not poor than that of Figure 2 (a). But when the electric field gets larger, the leakage current increases and the dielectric breakdown happens easily due to its poor step coverage characteristics.

Considering the characteristics of step coverage and the quality of silicon oxide, we optimized the deposition conditions of silicon oxide.

4. a-Si:H TFT characteristics

4.1 Initial TFT Characteristics

Bottom gate type TFTs were fabricated by 5 Mask process to investigate the effect of passivation layer on TFT characteristics.

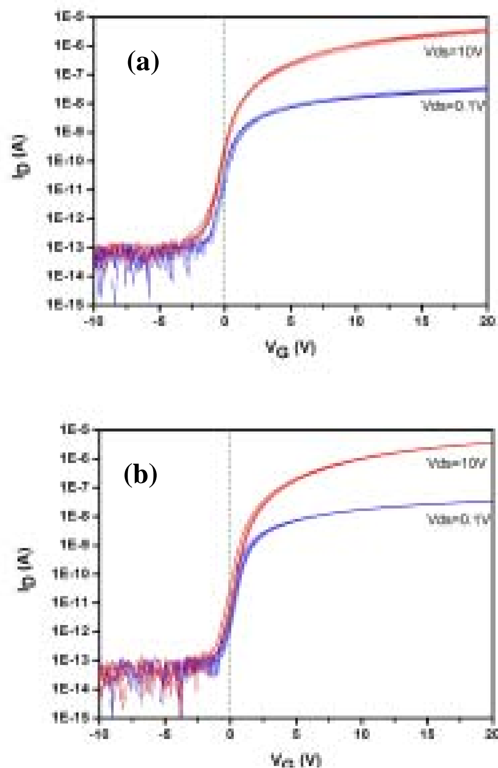

Figure 3. Transfer curves of TFTs
(a) Normal TFTs (SiNx passivation layer)
(b) TFTs with silicon oxide passivation layer

Table 1. Characteristics of TFTs in Figure 3

Pass. Layer	Ion (μA)	Mobility (cm^2/Vs)	V_{th} (V)	Subthreshold Swing (V/dec)
Normal (SiN_x)	3.5	0.49	0.26	0.50
Silicon oxide	3.7	0.54	0.81	0.49

Two types of TFTs were fabricated at the same time; TFTs with silicon oxide and silicon nitride passivation layer respectively. Figure 3 shows transfer curves of each type of TFTs. As is shown in Figure 3, two types of TFTs shows same characteristics. On current, mobility and subthreshold swing values are same for both types of TFTs considering its process and measuring variances.

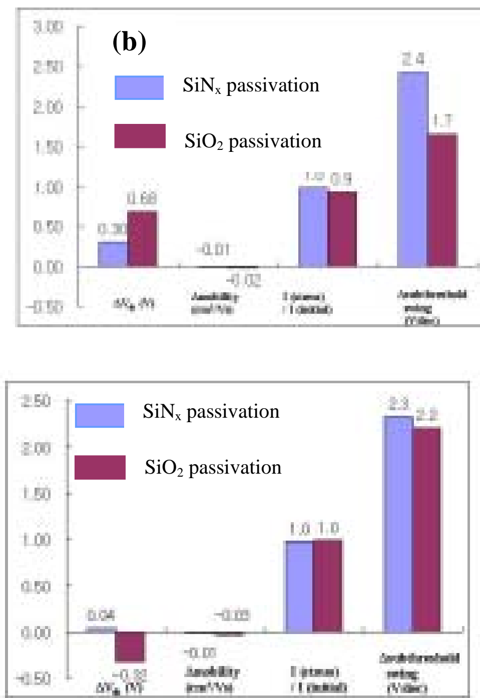

Figure 4. Changes in TFT characteristics by Gate bias stress
(a) Positive bias stress
(b) Negative bias stress

But threshold voltage values are somewhat higher in TFTs with silicon oxide passivation layer. The difference in the TFT characteristics would be come from the back channel state [3] because passivation layer deposition process can change the interface states at the back channel of TFTs. But threshold voltage difference between two types of TFTs is small so that it does not make any trouble in LCD panel driving.

4.2 TFT Characteristics after bias stress

Characteristics of TFTs after gate bias stress were measured. To apply gate bias stress, we applied ±30V on gate electrode for 1000s at room temperature. During applying gate bias stress, source and drain electrodes are grounded. The differences in TFT characteristics by gate bias stress were calculated after measuring. Figure 4 (a) shows the changes in transistor characteristics after positive bias stress. The change after negative bias stress is shown in Figure 4 (b). Although each parameter shows different values

between two types of TFTs, its difference are so small that it would not make any problems for LCD panel driving.

The real LCD panel with silicon oxide passivation layer was successfully fabricated. It showed no difference in image quality compared with normal LCD panels. The results on panel fabrication and its characterization will be presented in other conference soon.

5. Conclusion

Silicon oxide was adopted as passivation layer in a-Si:H TFTs to reduce the RC delay in high resolution LCD panels. The deposition conditions of silicon oxide were optimized considering its step coverage characteristics and current leakage characteristics. Then, the silicon oxide layers with low leakage current was adopted to a-Si:H TFTs to investigate the effect of silicon oxide on the characteristics of a-Si:H TFTs.

The device characteristics at initial state and changes in device characteristics by gate bias stress were investigated. And, it was shown that there was no difference in a viewpoint of device characteristics between two types of TFTs.

It was concluded that silicon oxide with our optimum conditions could be adopted instead of silicon nitride in a-Si:H TFTs in high resolution LCD panels with low RC delay.

6. References

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