

## Influence of the parasitic capacitance on pixel voltage drop of AMLCDs

**Suk-In Yoon, Sang-Ho Yoon**  
Sanayi System Co. Ltd., Incheon, Korea

**Chan-Yong Jung, Taeyoung Won**  
Dept. of Electrical Engineering, Inha University, Incheon, Korea

### Abstract

*In this paper, we report a novel method for extracting SPICE model for a unit cell of AMLCD. We investigated the influence of the parasitic capacitance on a pixel voltage drop of AMLCD. In this work, we generated a SPICE model for a unit cell of TFT-LCD by taking all of parasitic capacitances into account. In order to calculate the capacitance, we employed a finite element method. We calculated 21 capacitances including LC capacitance as a function of the applied voltage. In order to generate a SPICE model for LC capacitance, we used a piecewise linear voltage-controlled capacitor model with calculated values.*

### 1. Introduction

As the display size becomes larger, and the resolution higher, the image degradation effects such as flicker, crosstalk, and gray scale error become more important due to the incorporation of the TFT-LCD device parameters. Especially, the crosstalk resulting from the capacitive coupling among data lines, gate lines and pixel electrode through parasitic capacitors degrades an image quality severely in the large size TFT-LCD's. Therefore, Accurate SPICE model of TFT-LCD cell is required for the characterization of TFT-LCD<sup>[1]</sup>.

### 2. Capacitance Model of TFT-LCD

Because of the anisotropy of LC, capacitances in the TFT-LCD cell are affected by director distribution, that is, the capacitances are bias-and time-dependent. Therefore, in order to calculate capacitances accurately in the unit cell, we have

solved the Laplace equation and the Erickson-Leslie equation by a finite element method<sup>[2]</sup>. Thereafter, all of capacitances are calculated by using energy method<sup>[3]</sup>.

In this work, we have chosen a chevron type PVA mode as a test vehicle. Figure 1(a) and 1(b) shows the schematic overview and the capacitance equivalent circuit for unit cell of TFT-LCD. Referring to Figure 1(a), the exemplary TFT-LCD cell structure includes a total of 7 electrodes comprising two data lines, two gate lines, storage electrode, pixel electrode, and common electrode. Therefore, there are 21 unknown capacitance, 1 LC capacitance ( $C_{LC}$ ), 1 storage capacitance ( $C_{ST}$ ) and 19 parasitic capacitances. Referring to Figure 1(b), capacitances in this circuit model includes the parasitic capacitance between among a gate lines and a pixel electrode ( $C_{gp1}$ ,  $C_{gp2}$ ), the parasitic capacitance among data lines and a pixel electrode ( $C_{dp1}$ ,  $C_{dp2}$ ), the parasitic capacitance among data and gate lines ( $C_{gd11}$ ,  $C_{gd12}$ ,  $C_{gd21}$ ,  $C_{gd22}$ ), the LC capacitance  $C_{LC}$  and the storage capacitance  $C_{ST}$  only, and other parasitic capacitances are disregarded for their small capacitances. Furthermore, we have used Level 40 HP a-Si model for SPICE model of TFT<sup>[4]</sup> and piecewise linear voltage-controlled capacitor models for variable capacitances.

### 3. Simulation Results and Discussion

The calculated LC capacitance as a function of RMS (root mean square) voltage between pixel and common electrodes is shown in figure 2, and equation

<sup>1</sup> If necessary, you may place some address information in a footnote, or in a named section at the end of your paper.

(1) shows the piecewise linear voltage-controlled capacitor model for LC capacitance.

In the case of the other parasitic capacitances, they are the function of voltages because director of LC has moved differently under each voltage condition. However, since its variation has been less than 0.1% of its maximum value in MVA mode, they can be considered as the fixed value in this simulation. Figure 3 shows the supplied  $V_{G1}$ ,  $V_{G2}$ ,  $V_{D1}$ , and  $V_{D2}$  waveforms, conventional pixel inversion mode.

Figure 4 and 5 show the influence of data and gate lines which affects the pixel voltage. Referring to figure 4, the gate and pixel capacitance  $C_{gp1}$  increases amount of the kickback voltage  $\Delta V_p$  while the gate and pixel capacitance  $C_{gp2}$  decreases that of kickback voltage  $\Delta V_p$ . Furthermore, the signal of pixel electrode is ascending within ON state of next gate line. However, since turn on time of the gate signal has been relatively short, this effect can be negligible. Referring to figure 5(a) and figure 5(b), waveform of pixel electrode is fluctuated by the waveform of  $V_{D1}$ . Furthermore, in column inversion-like modes such as the pixel inversion mode or N-line inversion, the waveform of  $V_{D2}$  compensates the fluctuation of pixel signal. However, generally the waveform of  $V_{D2}$  is not matched that of  $V_{D1}$ , therefore, other driving methods which could compensate the fluctuation induced by the waveform of  $V_{D1}$  are required.

#### 4. Conclusions

In this paper, we have reported the influence of the parasitic capacitance on the pixel voltage drop of AMLCDs. In this work, we have generated the SPICE model for the unit cell of TFT-LCD using all

of parasitic capacitances. In order to calculate the capacitances, we have employed a finite element method. As a result, we have calculated 21 capacitances including LC capacitance as a function of the applied voltages. Furthermore, in order to generate SPICE model for LC capacitance, we have used the piecewise linear voltage-controlled capacitor model using the calculated values. Especially, we found that the capacitances  $C_{gp1}$ ,  $C_{dp1}$  increase the voltage drop of the pixel electrode while the capacitances  $C_{gp2}$ ,  $C_{dp2}$  decrease the voltage drop of the pixel electrode. Furthermore, the waveform of  $V_{D1}$  made the fluctuations of pixel signal while that of  $V_{D2}$  compensates those fluctuations. Therefore, further studies on the combination of  $V_{D1}$  and  $V_{D2}$  to compensate the fluctuations of pixel signal are required.

#### 5. Acknowledgements

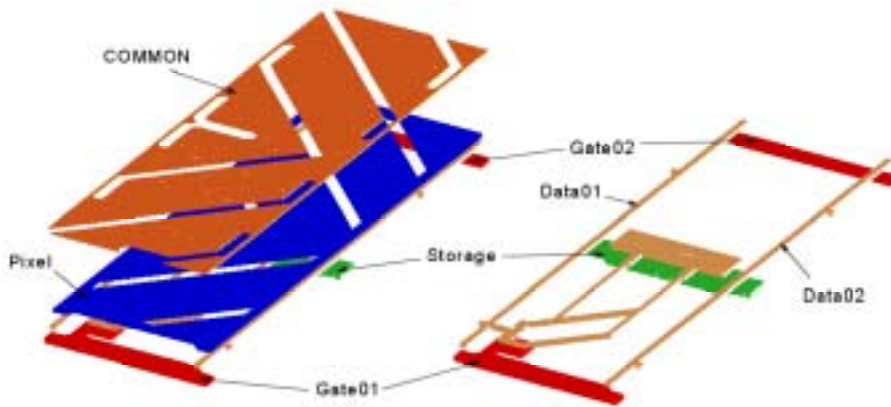
This work was supported by the Ministry of Information & Communication (MIC) of Korea through Support Project of University Information Technology Research Center (ITRC) Program supervised by IITA.

#### 6. References

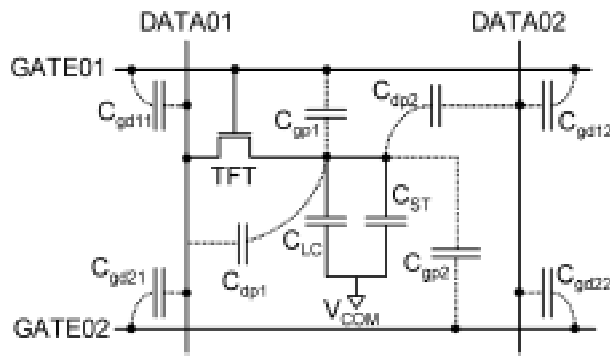
- [1] Y. Jeong, IEEE Trans. on Circuits and Systems, Vol. 44, No. 6, pp. 552-555, (1997).
- [2] C. Lee, Molecular Crystals and Liquid Crystals, Vol. 413, pp. 345-353, (2004).
- [3] S. Yoon, Journal of the Korean Physical Society, Vol. 40, No. 4, pp. 742-748, (2002).
- [1] H. Aoki, IEEE Trans. on Electron Devices, Vol. 43, No. 1, pp. 31-39, (1996).

$$\begin{aligned}
 & \text{Glc pixel common VCCAP PWL(1) pixel common} \\
 & + -6.50, 0.839843\text{p}, -6.00, 0.831120\text{p}, -5.50, 0.818794\text{p}, -5.00, 0.800529\text{p}, -4.50, 0.771693\text{p}, \\
 & + -4.00, 0.725919\text{p}, -3.50, 0.660901\text{p}, -3.00, 0.574530\text{p}, -2.50, 0.470439\text{p}, -2.00, 0.458021\text{p}, \\
 & + -1.50, 0.456107\text{p}, -1.00, 0.455356\text{p}, -0.50, 0.455022\text{p}, 0.00, 0.454946\text{p}, 0.50, 0.455022\text{p}, \\
 & + 1.00, 0.455356\text{p}, 1.50, 0.456107\text{p}, 2.00, 0.458021\text{p}, 2.50, 0.470439\text{p}, 3.00, 0.574530\text{p}, \\
 & + 3.50, 0.660901\text{p}, 4.00, 0.725919\text{p}, 4.50, 0.771693\text{p}, 5.00, 0.800529\text{p}, 5.50, 0.818794\text{p},
 \end{aligned} \tag{1}$$

+ 6.00, 0.831120p, 6.50, 0.839843p



(a)



(b)

Figure 1. SPICE Model : (a) schematic overview and (b) capacitance equivalent circuit for unit cell of TFT-LCD.

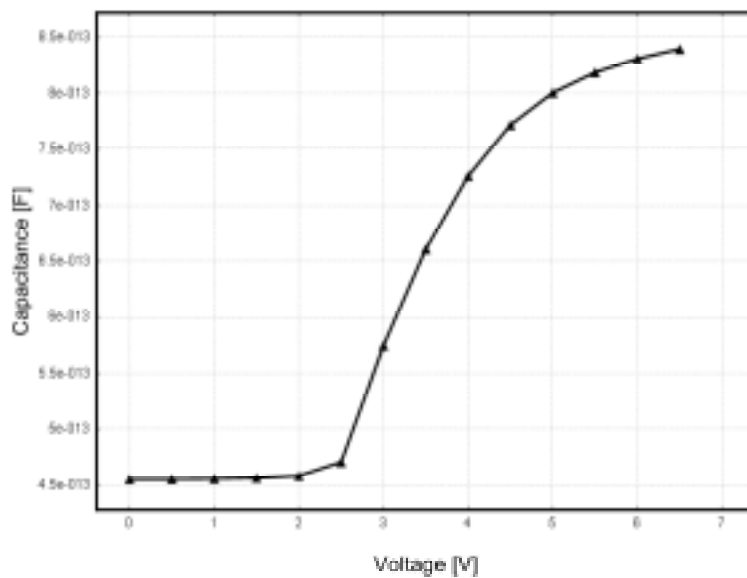


Figure 2. Calculated LC Capacitance vs. Voltage difference between pixel and common electrode.

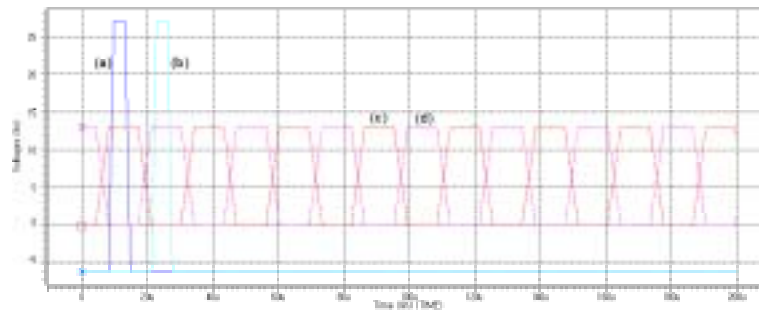


Figure 3. Supplied waveform: (a)  $V_{G1}$  (tied to GATE01), (b)  $V_{G2}$  (tied to GATE02), (c)  $V_{D1}$  (tied to DATA01), and (d)  $V_{D2}$  (tied to DATA02).

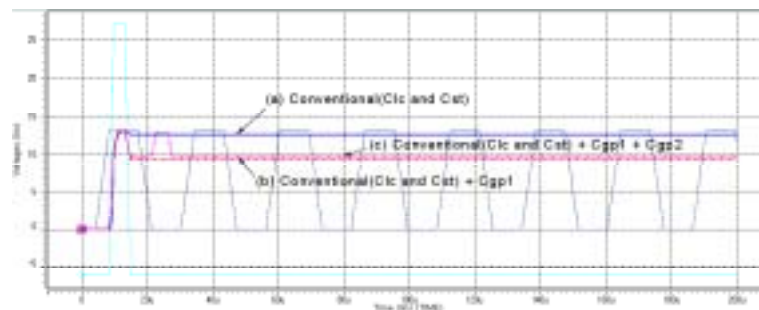
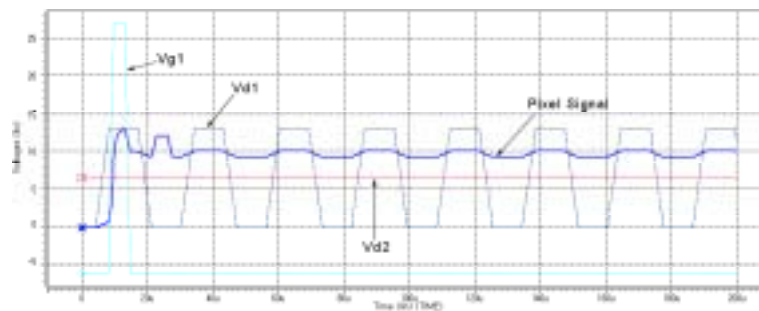
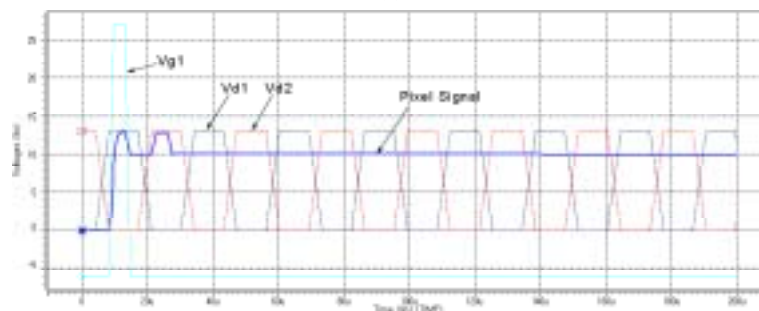


Figure 3. Influence of gate and pixel capacitances : (a) conventional ( $C_{LC}$  and  $C_{ST}$ ), (b) with gate01 and pixel capacitance, and (c) with gate02 and pixel capacitance.



(a)



(b)

**Figure 4. Influence of data and pixel capacitances : (a) with flatten  $V_{D2}$ , and (b) with oscillating  $V_{D2}$ .**