Topics in TFT device physics and modelling

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ABSTRACT

This paper contains a review of methods to analise static and dynamic properties of trap states in TFTs. The Gap Density of States is extracted from C-V and I-V characteristics. Switch on transients and small signal ac measurements are used in conjunction with simulation and an analytic model to extract traps dynamic parameters.

1. INTRODUCTION

The focus of this paper is the analysis of static and dynamic characteristics of traps in TFTs. Section 2 reviews a recent method for the extraction of the Gap Density of States (DOS). Section 3 discusses the transient behaviour of polycrystalline silicon TFTs and correlates it with the DOS and trap parameters. Small signal AC measurements and their use in the study of traps are presented in Section 4.

2. DETERMINATION OF DOS

The gap Density-Of-States (DOS) controls both static and dynamic properties of thin film transistors. It is therefore not surprising that this topic has been the subject of a number of investigations in the past two decades [1]. Among the proposed techniques, the field-effect method has become quite popular due to its apparent simplicity. In its simplest form, the method consists in deducing the surface field, F_S, as a function of surface potential, ψ_S, from the channel conductance (G) vs. gate-to-source voltage (V_{GS}) data. [2] The DOS, indicated hereafter by $N(E)$, is then calculated as $N(E) \approx \partial^2 F_S^2/\partial\psi_S^2$, where F_S and ψ_S are the surface electric field and the surface potential respectively. The problems involved in this approach are: (i) the flat band voltage V_{FB}, the bulk Fermi Energy E_F, the electron and hole contributions G_{n0}, G_{p0} to the flat band conductance G_0 are not known; this may result in an incorrect location of the $N(E)$ function along the energy axis; (ii) the 0 ^{o}K approximation for the Fermi function is assumed, which results in overestimating $N(E)$ especially near the band edges, where the slope of the DOS can be much higher than $1/kT$; (iii) the second derivative of F_S^2 magnifies any noise which may be present in the original data, making the extracted $N(E)$ inaccurate especially near mid-gap, where oscillations larger than one order of magnitude are observed. Reverse modelling, that is finding the $N(E)$ function which best fits the I_D-V_{GS} characteristics in 2-D simulations, has been also employed but it is time consuming and not without uncertainties due to other unknown parameters such as the flat band voltage V_{FB} and E_F. Furthermore, since thinner active layers (<100nm) are increasingly being employed for amorphous silicon (a-Si), polycrystalline silicon (poly-Si) TFTs and Organic TFTs (OTFTs), the effect of interface states is expected to be significant. The combination of I_D-V_{GS} and C-V measurements to determine both interface and bulk DOS was initially suggested in Ref.2. However, that method was based on the 0°K approximation, employed $N(E)= \partial^2 F_S^2/\partial\psi_S^2$ and was only applicable to the case of a semi-infinite active layer. We have developed a semi-analytical method that overcomes these

[1] See for instance: O K B Lui et al., J. of Appl. Phys., **89**, 6453, (2001) and references therein.

[2] T. Suzuki et al., Jpn. J. Appl. Phys., Part 2 **21**, L159, (1982).

problems, based on a recursive analysis of C-V and I_D-V_{GS} characteristics.[1] The surface potential vs. gate voltage (ψ_S-V_{GS}) relationship is obtained from:

$$\frac{d\psi_S}{dV_{GS}} = 1 - \frac{C}{C_{ox}WL}, \qquad (1)$$

where C is the measured low frequency capacitance between the gate and the combined drain and source contacts tied together and C_{ox} is the gate oxide capacitance. The V_{GS}-ψ_S relationship is obtained by integration of equation 1, provided the flat band voltage, V_{FB}, is known. We have shown that, under the assumption that both the bulk DOS $N(E)$ and interface state density N_{SS} can be considered constant near flat band, V_{FB} is given by the minimum in the low frequency C-V curve. The V_{GS}-ψ_S relationship so obtained is independent of the conductance-gate voltage (G-V_{GS}) data. The latter provides the additional relationship necessary to separate the interface states from the bulk DOS. The relationship among V_{GS}, ψ_S, the charge on the gate metal Q_G, the bulk charge Q_B and the surface charge Q_{SS} is:

$$Q_G = -Q_{SS} - Q_B = C_{ox}WL\left(V_{GS} - V_{FB} - \psi_S\right), \qquad (2)$$

where $Q_B = -\varepsilon F_s$, $F_S = -\left.\frac{d\psi}{dx}\right|_{x=0}$ and ε is the dielectric permittivity of silicon. Note that the $\psi(x)$ profile, where x is the co-ordinate perpendicular to the channel, $x = 0$ being at the gate-oxide semiconductor interface, has to be calculated in order to deduce Q_B. The $\psi(x)$ profile can be obtained from Poisson's equation:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon}\left[N_{trap} + n - n_0 - p + p_0\right] \qquad (3)$$

where:

n,p, are the electron, hole concentrations and n_0, p_0 indicate the equilibrium values;

$$N_{trap}(\psi) = \int_{E_V}^{E_C} N(E)\left[f(\psi) - f_0\right]dE; \qquad (4)$$

$$n(\psi) - n_0 = \frac{2N_C}{\pi^{1/2}(kT)^{3/2}}\int_{E_C}^{\infty}\left(E - E_C\right)^{1/2}\left(f - f_0\right)dE \qquad (5)$$

where E_C, N_C are the conduction band minimum and the effective density of states and T is the absolute temperature;

$$f\left(E, E_F + q\psi\right) = \frac{1}{1 + e^{\frac{E - E_F - q\psi}{kT}}},$$

and $f_0 = f(\psi = 0)$. An expression similar to equation 5 holds for $p(\psi)$-p_0.

The channel conductance, G, is given by:

$$G = \frac{G_{n0}}{d}\int_0^d e^{\frac{q\psi(x)}{kT}}dx + \frac{G_{p0}}{d}\int_0^d e^{\frac{-q\psi(x)}{kT}}dx, \qquad (6)$$

where G_{n0}, G_{p0} are the electron and hole equilibrium conductances, , and d is the active layer thickness. Starting from the experimental G_{exp}-V_{GS} characteristic, Equations 2, 3, 4, 5 and 6 can be solved self-consistently, according to the procedure described in Ref.1. To test the accuracy of the method, I-V and C-V characteristics for a poly-Si TFT were simulated using the ISE software. The DOS was then extracted and compared with the input DOS (Fig.1).

3. GATE SWITCH-ON TRANSIENTS

We reported previously[3] that poly-Si TFTs exhibit excess transient current, upon gate switch-on, referred to as transient overshoot. As shown in Fig.2, the overshoot decreases for decreasing time between pulses (T_{off}), and disappears for $T_{off} < 100\mu s$. A similar overshoot has been observed in SOI-MOSFETs.[4] The effect can be explained in the following way. When a positive voltage step is applied to the gate of a n-channel device, the body floats positive with respect to the source, forward biasing the source-to-body junction.

[3] N Bavidge et al, Appl. Phys. Lett.,**77**, 3836, (2000).
[4] H.C. Shin et al., IEEE Trans. Electron Devices., **43**, 318,(1996).

The steady-state is achieved through electron injection from the source into the body. Some of these electrons are driven towards the interface to form the conductive channel (charge per unit surface Q_n), the rest recombine with the background holes, giving rise to the depletion region (charge per unit surface Q_B). The latter process requires a finite time, as the current through the source/drain body junctions is limited. Since $Q_n+Q_B \approx C_{ox}V_{GS}$, if $Q_B(t) < Q_B(\infty)$ then $Q_n(t) > Q_n(\infty)$ and an excess drain current is observed. Since the source-body recombination current is inversely dependent upon the carrier lifetime τ, and the number of holes to be recombined is proportional to the acceptor concentration N_A, the transient time increases with τ and N_A. If the SOI-MOSFET is fully depleted, the transient becomes extremely short. In poly-Si the carrier lifetime is of the order of nanoseconds and the active layer is intrinsic. Therefore, one expects very fast transients. By contrast, we observe transients lasting several milliseconds. Fig.3 shows experimental and simulated transients for V_{DS} =0.1V and V_{GS} stepped from 0 to 7V. The simulations were performed with the ISE simulator, by using the extracted DOS and assuming acceptor-like (donor-like) states in the upper (lower) half of the bandgap. Energy dependent capture cross-sections were employed and the best fit spectrum is shown in Fig.4. The different behaviour of poly-Si TFTs compared to single-crystal SOI is due to the fact that poly-Si is undoped (Fermi level near the mid-gap), so the formation of the depletion region proceeds through capture of electrons into initially empty states, rather than through recombination of free holes. Under these conditions, the transient consists, for n-channel devices, of contributions from all acceptor-like traps in the upper half of the bandgap: the tail states, with a larger capture cross section, are responsible for the fast transient portion (not shown), whereas the deep states, with smaller cross sections, give rise to the long transient shown in Fig.2. In between pulses, electrons are emitted from the traps, but for small T_{off}, the time slot is insufficient to reach the equilibrium condition, corresponding to the Fermi Level lying near midgap. Therefore, at the start of the next pulse the traps are already full of electrons. Hence $Q_B(t) \sim Q_B(\infty)$, $Q_n(t) \sim Q_n(\infty)$ and no overshoot is observed. It is worth noting that the overshoot is reduced when the trap density is reduced. This is for instance the case of single-grain TFTs, particularly in the devices with high mobility (~400 $cm^2V^{-1}s^{-1}$). It is interesting to examine the overshoot dependence upon V_{DS}, shown in Figs. 5.[5] The excess current increases with V_{DS} up to 3.5 V. Beyond that it decreases until, for V_{DS} = 10V an undershoot occurs. It is evident from the inset of Fig.5 that the decrease of the excess current corresponds to the onset of the kink. The effect can therefore be explained by the presence of two competing processes: electron capture and hole capture by traps. Holes are generated in the high field drain region and eventually dominate the trap kinetics, owing to the larger hole cross section of the acceptor states, resulting in an undershoot.

4. AC ANALIYISIS

This is an alternative technique to study the TFT dynamic performance. A small AC signal is superimposed to the DC gate voltage and the AC current is detected at the source through a lock-in amplifier. In order to describe the principle of this technique, we will assume that the ac response is controlled by a single trap level. A simple model[6] is presented below. For a n-channel device, the response can be described by the following 1st order differential equations:

[5] N Bavidge, PhD Thesis, Cambridge University, (2002).
[6] F Yan et al, Appl. Phys. Lett., **82**, 2062 (2003).

$$q\frac{d(n(t)+N_T^-(t))}{dt}=C_v\frac{dV_{GS}}{dt}$$

$$\frac{dN_T^-(t)}{dt}=\frac{n(t)}{\tau_c}-\frac{N_T^-(t)}{\tau_e} \quad (7)$$

where $n(t)$ is the number of free electrons in the conductance band, $N_T^-(t)$ is the number of electron occupied traps, τ_c is the average capture time and τ_e is the average emission time; q is the electron charge; C_v is the capacitance of the TFT at a gate voltage V_{GS}. Since the conductance of the channel is proportional to the number of free electrons, solving for $n(t)$ we have for the real and imaginary components of drain current and impedance:

$$i_{\mathrm{Re}} \propto \frac{\tau/\tau_e+\omega^2\tau^2}{1+\omega^2\tau^2}=1-\frac{\tau}{\tau_c}\frac{1}{1+\omega^2\tau^2}$$

$$i_{\mathrm{Im}} \propto \frac{\omega\tau}{1+\omega^2\tau^2}(1-\frac{\tau}{\tau_e})=\frac{\tau}{\tau_c}\frac{\omega\tau}{1+\omega^2\tau^2} \quad (8)$$

$$Z_{\mathrm{Re}} \propto 1+\frac{\tau_e}{\tau_c}\frac{1}{1+\omega^2\tau_e^2}$$

$$Z_{\mathrm{Im}} \propto -\frac{\tau_e}{\tau_c}\frac{\omega\tau_e}{1+\omega^2\tau_e^2} \quad (9)$$

where: $\frac{1}{\tau}=\frac{1}{\tau_c}+\frac{1}{\tau_e}$ (10)

The time constant τ can be determined from the peak frequency of i_{Re}, ω_{p1}, $\tau=1/\omega_{p1}$. The emission time constant τ_e can be calculated from the peak frequency of Z_{Re}, ω_{p2}, $\tau_e=1/\omega_{p2}$. So the capture time constant τ_c can be calculated from $\tau_c=\frac{1}{1/\tau-1/\tau_e}$. The half width of the relaxation peak of Z_{Im} in log axis is: $\log\omega_1-\log\omega_2=\log(7+4\sqrt{3})=1.144$. The treatment can be extended to the case of a distribution of trap levels and capture-emission time constants. In such case the peak will be broadened and eventually will disappear altogether, depending on the time constants distribution.

As shown in Fig.6, the imaginary component of the AC current of a poly-Si TFT shows a resonance peak with a corresponding step in the real component. The bias voltage applied on the gate was V_g=4.8V. The peak frequency is f_{p1}=147 Hz. The half width of the peak is $\log(\omega_1/\omega_2)\approx1.1$. We conclude that the resonant process is dominated by a single trap level. Fig. 7 shows the imaginary and real components of Z for the same measurement. The peak frequency of Z_{Im} is f_{p2}=87.2Hz. The calculated time constants are: τ_e=1.8ms, τ=1.1ms. From equation (10) τ_c=2.7ms.

When the gate bias is changed from 4.4 V, which corresponds to the flat band voltage, to 8.0V, the peak frequency f_{p1} and f_{p2} remain the same. However, the peak height undergoes a big change. As shown in fig. 8, the peak increases for $V_{GS}<6.5$ V, it has a maximum for V_{GS}=6.5V and then decreases with the increasing voltages, eventually disappearing for $V_{GS}>8.0$V. The gate voltage dependence of the peak height can be explained by considering the distance in energy between the dominant trap and the Fermi Level at the surface E_F. At low V_{GS}, E_F lies below the trap level and becomes closer to the latter for increasing V_{GS}. This results in a larger modulation of the electron population and in a higher peak. A maximum is reached for the V_{GS} value at which E_F crosses the trap level. After that, the trap is progressively filled with electrons and the peak height decreases. The surface potential value, ψ_S, corresponding to the maximum gives an estimate of the trap energy. The ψ_S-V_{GS} relationship can be extracted from low frequency C-V_{GS} measurements using equation 1. A plot of the peak height vs. ψ_S is shown in Fig 8 together with the C-V_{GS} data (inset). From this plot we locate the trap level at E_{F0}+0.35eV. From the flat band conductance $E_{F0}\sim E_V$+0.56eV. From the trap emission time τ_e we estimate the capture cross section $\sigma_n=3.1\times10^{-21}cm^2$ and,

from the capture time τ, the trap concentration N_T=5.7x 10^{15} cm^{-3}. The presence of traps centred near this energy has been reported before as a result of bias stress in poly-Si TFTs [7] and single crystal MOSFETs, [8] or radiation damage.[9]

6. CONCLUSIONS

We have reviewed methods for the analysis of static and dynamic properties of traps in TFTs. The DOS has been extracted by a new recursive analysis of C-V and I-V characteristics, resulting in improved accuracy and speed compared to previous methods. The gate switch-on transients in poly-Si TFTs have been employed, in conjunction with transient simulation, to extract the dependence of the traps capture cross section upon energy. Small signal AC measurements and an analytic model have been presented, providing additional characterization tools for traps in these devices.

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[7] G.Fortunato et al., IEEE Trans. Electron Dev **41**, 340,1994.

[8] S. K. Lai, Appl. Phys. Lett. **39**, 58, 1981.

[9] T.P.Ma et al., Appl. Phys. Lett. **27**, 61, 1975.

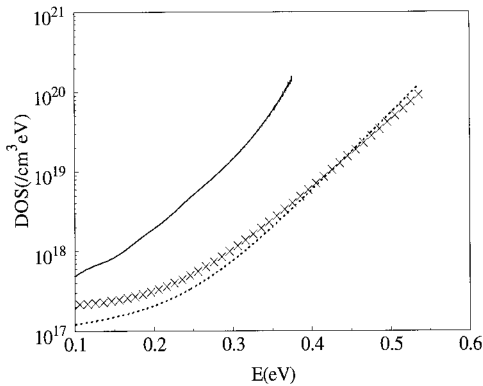


Fig.1 Comparison between input DOS (×) and extracted DOS for the present method (···) and for the old field-effect conductance method (—)

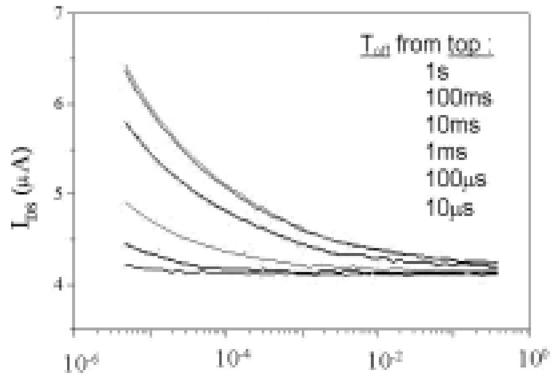


Fig.2 Overshoot dependence on T_{off}; V_{GS}^{+}=7V, V_{DS}=0.1V,

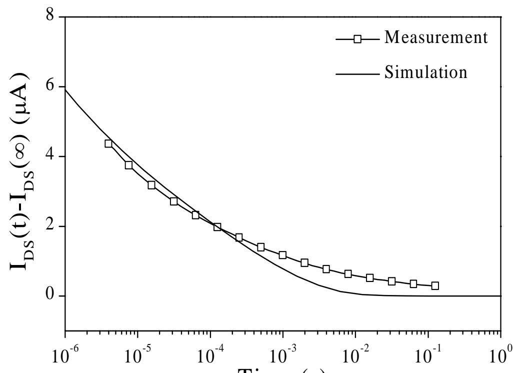


Fig.3 Comparison of experimental and simulated

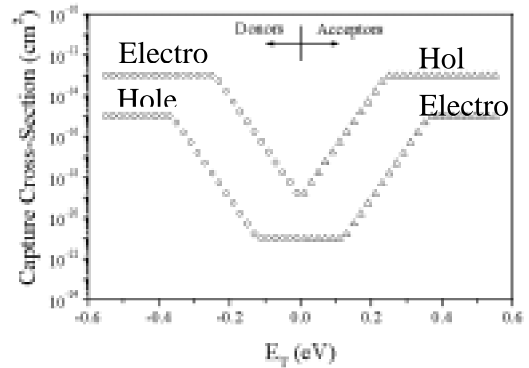
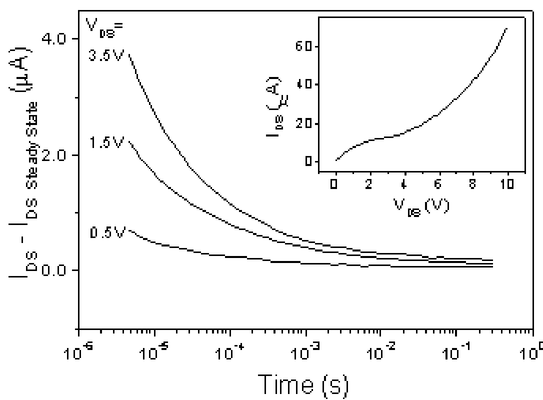


Fig. 4 Best fit capture cross sections for electrons and holes as a function of trap energy



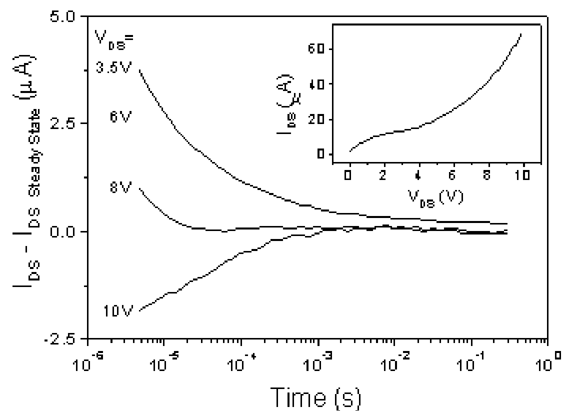


Fig.5 Overshoot dependence upon V_{DS}, for V_{GS}=0-7V. Left:V_{DS}=0.5V,1.5V, 3.5V; Right: V_{DS}=3.5V,6V, 8V, 10V.

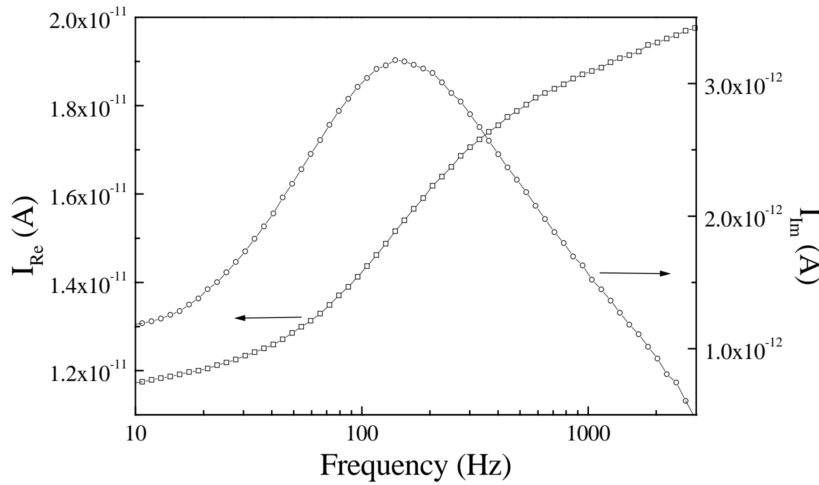


Fig.6 Real and imaginary components of ac source current. V_{GS}=4.8V, V_{DS}=0.01V

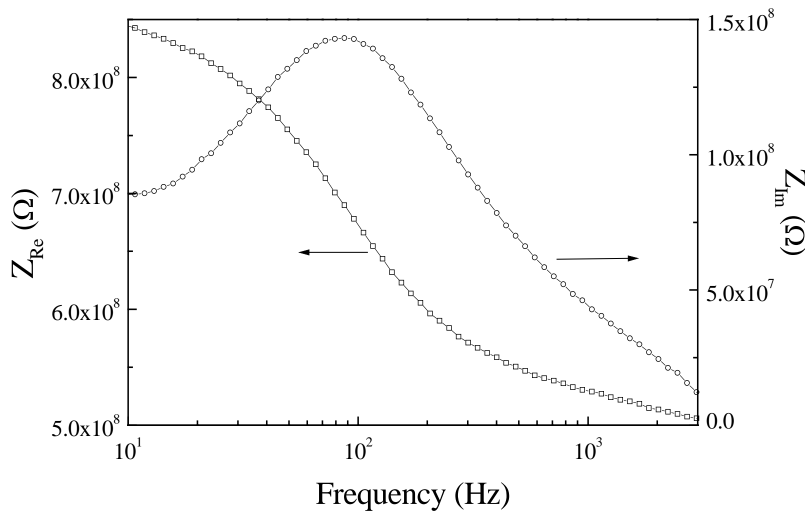


Fig.7 Real and imaginary components of the impedance . V_{GS}=4.8V, V_{DS}=0.01V

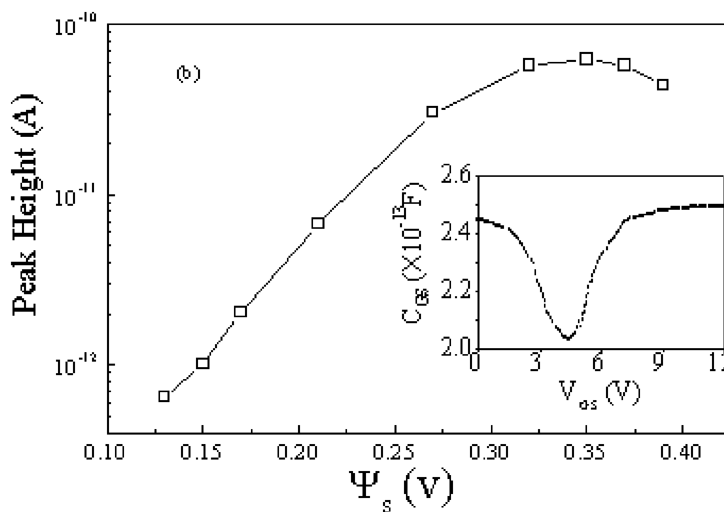


Fig.8 Height of the resonance peak of Fig. 6 vs surface potential Ψ_S. The surface potential has been deduced from the C-V measurements in the inset, using equation 1 in