Analysis of Row and Column Lines in TFT-LCD panels with a Distributed Electrical Model

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ABSTRACT

As the TFT-LCD panels become larger and provide higher resolution, the distributed capacitive and resistive lines induce the propagation delay, reduce the TFT-on time and deteriorate the pixel charging-ratio. A number of the compensation methods, like the H-LDC (Horizontal Line Delay Compensation), have been proposed to compensate the propagation delay of the large and high resolution panels [1]. These methods, however, require the comparatively accurate gate propagation delay estimates at each column driver. In this paper, by observing the actual gate and data waveform from 15-inch XGA TFT-LCD panels, we could predict the propagation delay along the row and column line.

1. Background and History

In TFT-LCD panels, a row signal from a gate driver IC turns on the TFT of a pixel and a column signal from a column driver IC charges up a storage capacitor and rotates liquid crystal. Signal delay in the row line affects pixel data, because the unwanted data comes into pixel. To solve this problem, the row line signal is shortened by the amount equal to the propagation delay time in the conventional method. The method, however, reduces the TFT-on time in each line and may not give enough time to transfer the data from the column driver to a TFT's LC capacitor. The H-LDC (Horizontal Line Delay Compensation) that the column line signal is also delayed by the delay time of the gate line is proposed to compensate the delay time [1]. This method can be implemented in the PPDS™ (Point-to-Point Differential Signaling) architecture introduced by National Semiconductor [2]. In order to realize the H-LDC driving method, it is important to know the exact RC delay waveform in the actual TFT-LCD panels.

It can be assumed that a row/column line is a transmission line which is composed of resistors and capacitors. The transmission line can be made by a simple lumped model or a distributed model. The simple lumped RC model is inaccurate for a long wire like the gate lines and the data lines in the TFT-LCD panel. For these wires, the distributed RC model is more appropriate [3]. To save the simulation time and avoid the complexity of the model, it is more desirable to combine resistors and capacitors from each pixel into the several blocks that result in the optimized distributed model.

This paper is focusing on the RC delay in a 15-inch XGA TFT-LCD (Samsung) panel and the resistance and capacitance from the structure of the panels using tools such as Auto CAD and SPICE LINK. We optimize the row/column distributed line and compare the measured RC waveform with HSPICE simulation results. It takes into accounts not only the capacitance from the structure of the panels but also the capacitance due to process variation of panels by tracking the measured waveform. Through this procedure, we can predict the propagation delay in the middle of each line as well as the delay at the end of the line.

2. The Row/Column Line Distributed Model

The row/column line in the TFT-LCD panel can be modeled by RC distributed model. One lumped T model consists of 2 resistors and 1 capacitor like the block in Fig. 1. If the unit pixel in the 15-inch XGA (1024*768) TFT-LCD panel is one lumped T model, one row (gate) line consists of 6144 resistors and 3072 capacitors. There are 1536 resistors and 768 capacitors in one column (data) line. In one simple lumped T- model, one row/column line is made up of 2 resistors and 1 capacitor. If the row/column line, like the line in the TFT-LCD panel, becomes longer, there's some significant errors in one simple lumped model. Therefore we have to consider the distributed

model which is composed of several lumped models. It is needed to research how many blocks are acceptable and accurate.

As shown in Fig.1, the row/column line can be considered as the distributed model which is made up of N blocks. The bigger the number of N becomes, the closer waveform from this model is to the measured waveform. But it is not necessary for blocks to be divided by 1024 in the row line and 768 in the column line. The optimized distributed model can be found out through HSPICE, increasing N. Through the simulation, 16 blocks in the row line and 12 blocks in the column line are appropriate.

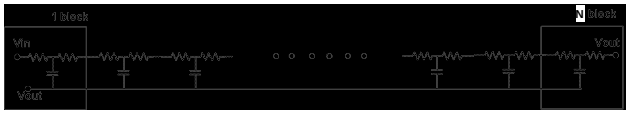

Fig. 1 N-distributed T model

3. Measurement of RC Delay

How can we probe the waveform and the propagation delay from the actual panel of the row/column line? While measuring the RC delay with the panel on, it is essential to manipulate the panel. At first, LCM (LCD Module) is separated into the backlight part, the panel part, and the gate/data driver IC exposed like Fig. 2.

The gate/data input waveform from each driver IC can be measured on the white circle pattern in Fig.2. To measure the gate/data output, the delayed waveform at the end of the line, the panel should be done by laser-shorting and the gate/data line in the panel of back side corner like Fig. 2 should be manipulated.

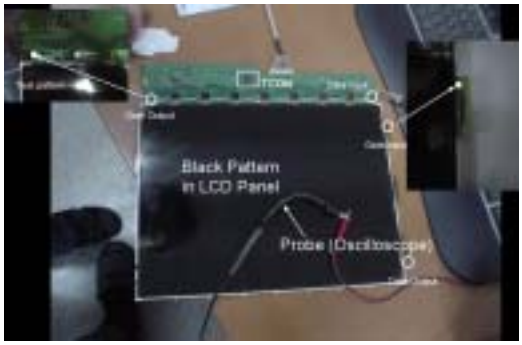

Fig. 2 TFT-LCD Panel for measuring RC Delay

By probing the panel, gate/data input and gate/data output, gate OE signal and clock are measured. It can be used that the clock and the gate OE signal are reference signals data for triggering the accurate waveform and adjusting the waveform. Through this measurement, the measured waveforms are as follows.

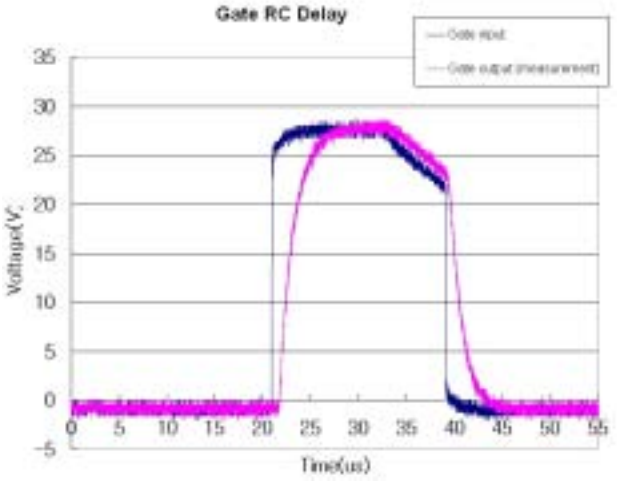

Fig. 3 Gate line Waveform (Gate input and Gate output)

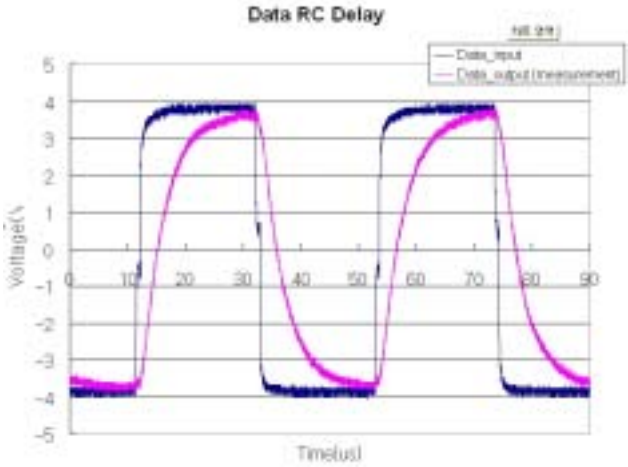

Fig. 4 Data line Waveform (Data input and Data output)

4. Extraction of Resistance and Capacitance Value from the Unit Pixel

It is too difficult to measure resistance and capacitance in one pixel directly, because it has micro-meter size and complex structures. The structure of unit pixel should be known. If the micro structure can be observed, resistance and capacitance value will be extracted through the following procedures.

At first, the method that we choose is to separate the panel part into the TFT part and the color filter

part. The structure of pixels in the TFT part can be observed and measured through the microscope. Secondly, the 2-dimensional structure in Fig.5 is drawn by Auto CAD and changed into the 3-dimensional structure in Fig.6 by SPICE LINK, considering thickness of each layer. After putting material properties of layers into SPICE LINK and doing the 3-D simulation, the resistance and the capacitance in Table 1 are obtained. Applying the resistance and the capacitance to the optimized distributed model, the simulation waveform will be compared with the measured waveform.

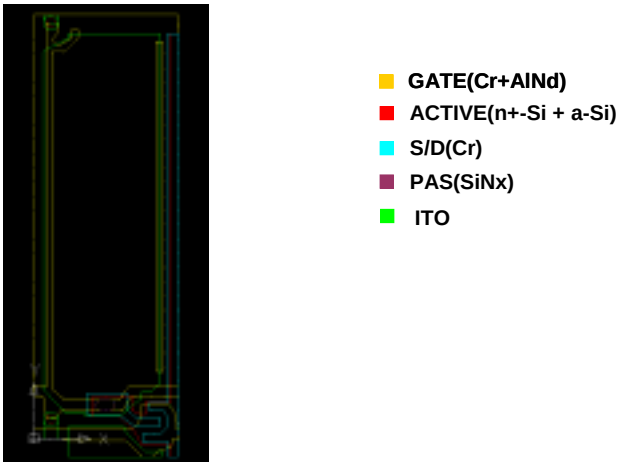

Fig. 5 2D structure of unit pixel by Auto-CAD

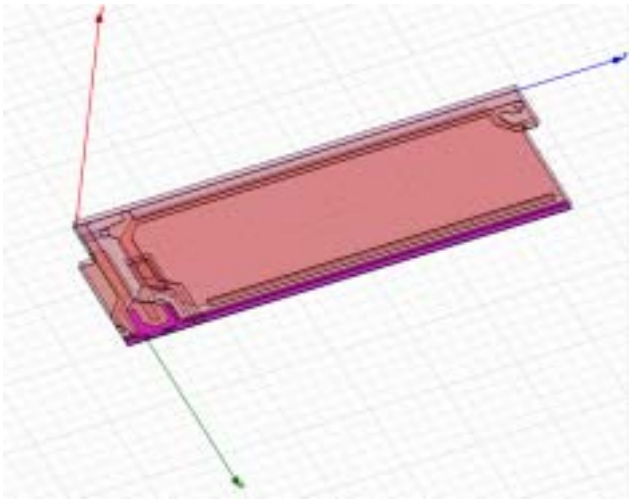

Fig. 6 3D structure of unit pixel

6. Comparison of the SPICE Simulation Results and the Real Waveform

HSPICE simulations in the row/column line, based on the resistance and the capacitance in Table 1 and the appropriate distributed model above, are completed.

	Line	Results per unit pixel	Results per line
Resistance	Row[Gate]	2.16Ω	6.64 kΩ
	Column[Data]	53.19Ω	40.85 kΩ
Capacitance	Row[Gate]	0.1184pF	363.7pF
	Column[Data]	0.157pF	120.7pF

Table 1 Results of 3D simulation

This simulation results are compared with the measured waveform. The difference between two waveforms emerges. The reason that the different waveforms come out is to exist in process variation. Especially the resistivity of thin film is sensitive to the thickness and deposition temperature. The thinner thickness of thin film is, the bigger resistivity of it becomes [4]. It is assumed that the capacitance is reasonable because the value is obtained by observing structure of unit pixel and the accuracy of 3D simulator is verified in interconnect capacitance estimation [5]. The resistivity of AlNd (5 uΩ*㎝) and Cr (21uΩ*㎝) was used. Based on the variation of resistivity, we fixed the capacitance value and varied the resistance of each line.

The appropriate value is obtained in table 2. The resulting resistance values of each line are 8.4kΩ and 49kΩ. These values are greater than ones from 3D simulation by 20% and 27% each. The difference can be compensated using the fitting factor. Average fitting factor (γ) is 1.24(=1.20+1.27)/2). Extracting the resistance and capacitance from the 3D simulation and multiplying each resistance by 1.24, the more accurate RC delay has been acquired. This fitting factor could be applied to other application models. The simulation results where fitting factor is applied are shown in Fig.7 and Fig.8.

	Line	Results per line(3D simulation)	Results in tracking value
Resistance	Row[Gate]	6.64 kΩ	8.4 kΩ
	Column[Data]	40.85 kΩ	49 kΩ
Capacitance	Row[Gate]	363.7pF	363.7pF
	Column[Data]	120.7pF	120.7pF

Table 2 Comparison of 3D simulation value with value in tracking (RC value)

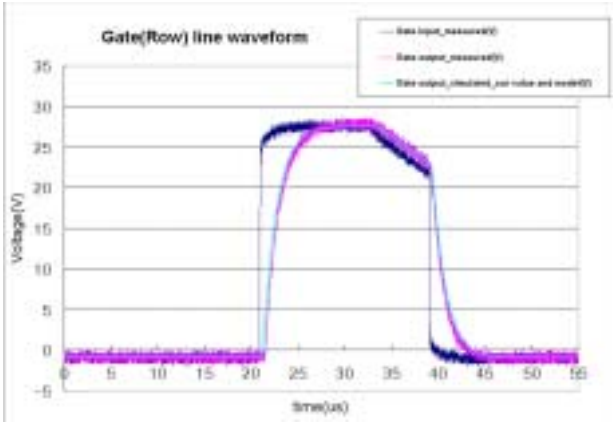

Fig. 7 Comparison of measurement results with 3D and HSPICE simulation results in Row line

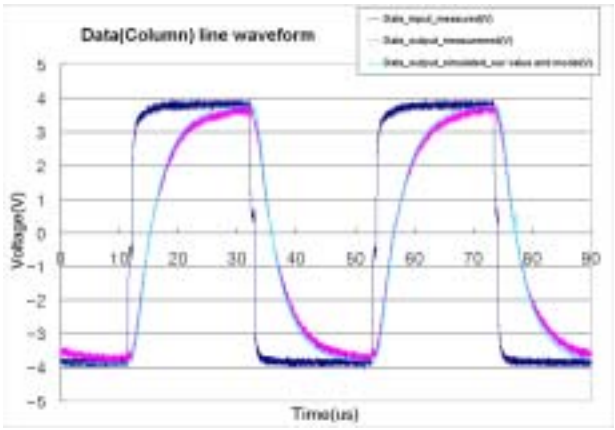

Fig. 8 Comparison of measurement results with 3D and HSPICE simulation results in Column line

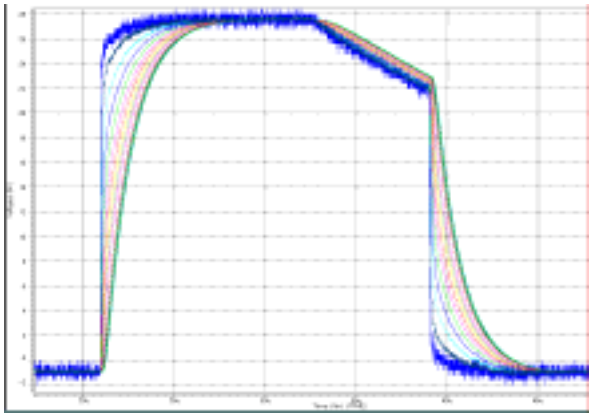

Fig. 9 HSPICE simulation results of the row line delay at the end of each block

8. Conclusions

The more accurate capacitance that includes the static and the dynamic characteristics can be obtained through the direct measurement of the waveform in the actual TFT-LCD panel. Choosing the appropriate N distributed model, the RC delay time at each node also can be expected without measuring the RC delay in Fig.9. This RC time delay analysis of the row/column line is fundamental to applying the H-LDC(Horizontal Line delay compensation) to PPDS^{TM}(Point-to-Point Differential Signaling). Because the column line signal should be delayed according to the amount of the row line delay, knowing the RC delay at each node without measuring is very important. The exact delayed column signal can expand the charging time of pixel. It means that TFT-LCD panel can provide the high quality image. Through observing the structure, doing the 3-D simulation, and doing SPICE simulations simply, the more accurate waveform and propagation delay time can be obtained easily. The larger TFT-LCD panels become, the more important expecting the RC delay time in each line is. Predicting the exact delay time in large size LCD TVs will be essential to increase the charging ratio and give a chance to provide clearer and higher quality image.

9. Acknowledgment

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10. Reference

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