Recent Progress in Low Cost Dual-Select-Diode AMLCD Technology

Willem den Boer and G. Scott Smith
ScanVue Technologies LLC, Hillsboro, Oregon, USA
willem@scanvuetech.com

Abstract
Recent developments in Dual Select Diode (DSD) AMLCD technology are described. They include a novel array design and drive method with shared select lines, which leads to higher aperture ratio and a further reduction of module cost. A Color-On-Array DSD process and pixel layout compatible with In-Plane-Switching is also proposed.

1. Introduction
The Dual Select Diode (DSD) AMLCD has been proposed as a low cost alternative to a-Si TFT LCDs and has 20% lower module manufacturing cost and 60% lower capital investment for the array process [1,2]. In earlier papers we reported on prototype 10 in. VGA DSD AMLCDs and on improved drive methods eliminating cross- talk [3,4,5]. The DSD AMLCD can be manufactured with only two or three mask steps in the array process, with relaxed design rules [6]. It was also shown by SPICE simulations that DSD AMLCDs can be scaled up to large area exceeding 40 inches in diagonal size [1,3].

The conventional DSD AMLCD has two select lines for each row of pixels. This necessitates doubling of the number of row driver connections and the use of row driver chips with twice the number of output channels. Such a row driver, with the optimized offset-scan-and-hold drive method, has been developed by Novatek Microelectronics [7]. Although the overall cost of the LCD module is not affected much by the additional row driver connections and output channels, there is a small loss of aperture ratio and manufacturing yield associated with the presence of two adjacent select lines at each pixel row. In this paper we describe an alternative pixel circuit and drive method, in which the select lines between two adjacent rows of pixels are shared. This reduces the number of row driver connections to the same number as in TFT LCDs and also improves the pixel aperture ratio.

Another issue with the DSD AMLCD is that the original process and layout is not directly compatible with the In-Plane-Switching (IPS) LC mode to enhance viewing angles. In this paper we also propose an alternative DSD process and pixel design which utilizes the IPS mode.

2. The shared select DSD pixel circuit
In the Dual Select Diode (DSD) AMLCD each pixel consists of a differential circuit with two equal nonlinear resistors or TFDs (Thin Film Diodes). The nonlinear resistors can be SiNx diodes in which the N to Si ratio x in the film can be tailored to obtain the appropriate ON and OFF current as shown in figure 1.

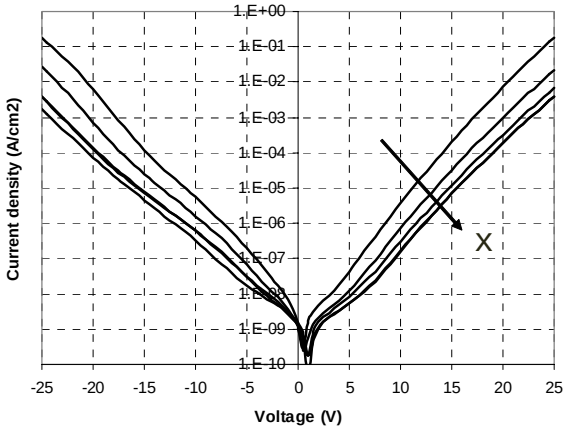

Figure 1. Measured characteristics of SiNx diodes with varying N/Si ratio x and SiNx thickness of 200 nm

When sufficient voltage is applied across the nonlinear resistors, they conduct and bias the pixel electrode accurately to $(V_{s1}+V_{s2})/2$ (see figure 2).

After the voltage on the select lines is subsequently reduced to zero, the diodes no longer conduct and the voltage node between the diodes becomes floating. The data voltage applied to the opposite electrode of the LC capacitor on the color plate (not shown in figure 2) is then accurately stored on the pixel. The DSD pixel circuit gives superior gray scale control as compared to a circuit with a single TFD, since the

differential circuit of the two nonlinear resistors cancels out TFD variations across the display area and over time and temperature [1,2]. The DSD circuit also cancels out RC delays on the buslines to a large degree and therefore allows scale-up to large display size [1,3].

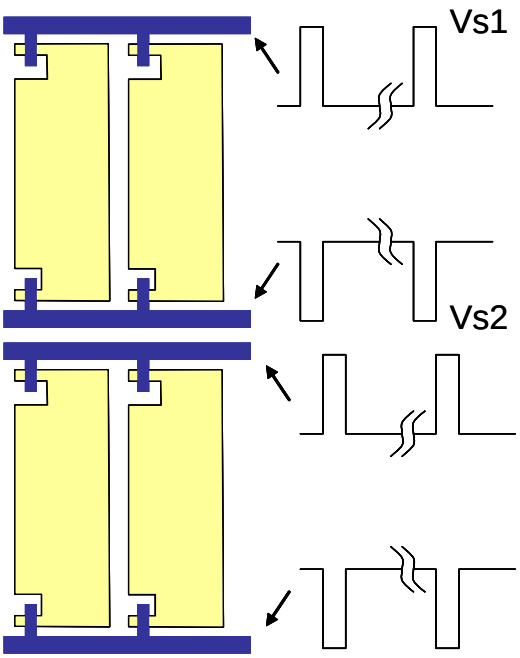

Figure 2. Pixel layout and select pulses for four pixels in DSD array with separate select lines

In the conventional DSD pixel array each row of pixels has its own dedicated set of two select lines, reducing aperture ratio and requiring two row driver outputs for each row of pixels.

In figure 3 and 4 an alternative layout, pixel circuit and drive method are shown with shared select lines [8]. In this configuration the opposite polarity select pulses for each row overlap by approximately one line time. A row is selected when both adjacent select lines are simultaneously selected. For example row i is selected in the time interval between t2 and t3 and row i+1 is selected in the time interval between t3 and t4. The non-select voltage on the rows is 0 and the data voltage applied to ITO stripes on the opposite substrate alternates from line to line between 0 to 5 V and 0 to -5 V (full range line inversion). It can be shown by circuit modeling that, with the correct polarity of the line inversion drive, the leakage through the diodes on row i is negligible during selection of row i+1, even though S_{i+1} is still selected. At time t3, when row i is deselected and row i+1 is selected, the data line voltage is inverted from positive to negative voltage. This pulls down all the pixel electrode voltages on non-selected rows. The resulting voltage across the diodes on row i that are connected to S_{i+1}, is sufficiently low to prevent any leakage during the following line time when row i+1 is selected, as confirmed by SPICE simulations.

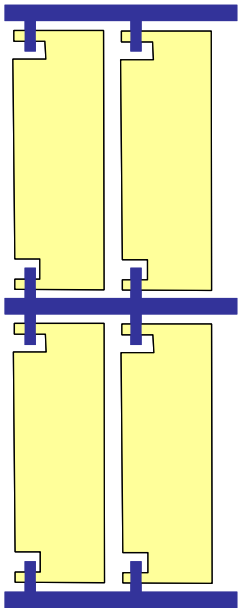

Figure 3. Pixel layout of four pixels in DSD array with shared select lines

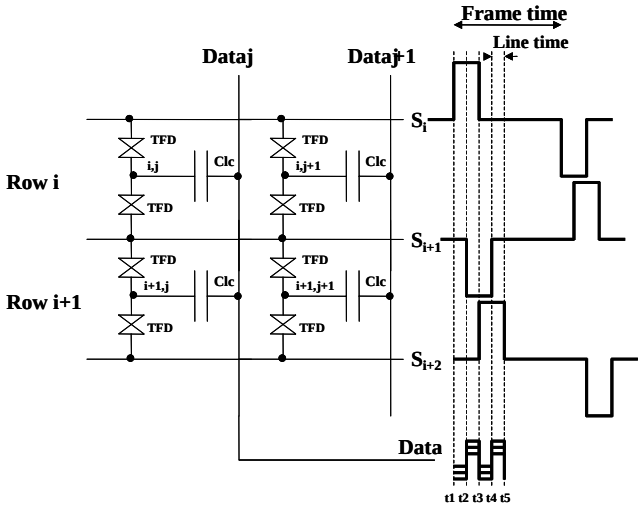

Figure 4. Pixel circuit and drive scheme of four pixels in DSD array with shared select lines

In this shared select drive scheme it is essential that the select voltages and data voltage change at the same time to avoid diode leakage. This method is therefore less compatible with large displays in which the turnoff of the select voltage varies along the row line as a result of RC delays. It is, however, compatible with small displays with negligible propagation delays of the select pulses.

In addition to reducing the number of row driver output channels, the shared select drive scheme also improves aperture ratio, as follows from comparing figures 2 and 3, and increases yield by eliminating the possibility of shorts between adjacent select lines.

3. IPS compatible DSD process and layout

The color plate in AMLCDs represents a significant part of the total manufacturing cost, between 10 and 15% of the final module cost. To reduce cost of the counter substrate and to maximize aperture ratio, the Color-On-Array (COA) TFT LCD was proposed a number of years ago [9]. By patterning the color filters on the active array substrate, the counter substrate can be very simple, without any patterning steps. This eliminates the need to accurately align the active and counter substrates during LC assembly. In a-Si TFT LCDs, however, the COA approach increases the number of patterning and process steps on the active array to eight or more [10] and has a negative impact on the manufacturing yield. Therefore, the COA method has not been widely adopted. In DSD AMLCDs the number of mask steps on the active array can be as low as two and adding the color filters will increase the number to only five. DSD AMLCDs with COA and the TN mode of operation have been proposed earlier, using simple ITO data lines on the counter substrate [11].

In this paper a variation on the COA DSD AMLCD is proposed, which is specifically designed for In-Plane-Switching [12]. Figure 5 shows the proposed process step by step along with the pixel layout. A metal layer and SiNx layer are sequentially deposited and patterned together to form the select lines and the bottom electrode and insulator for the diodes and storage capacitance. Then the red, green and blue color filters are patterned with openings at the diode and storage capacitor locations. Finally, the top metal is deposited and, with the fifth patterning step, delineated into data lines, top electrodes for the diodes and storage capacitor and grid electrodes for the IPS mode. The counter substrate is plane glass without any film or pattern.

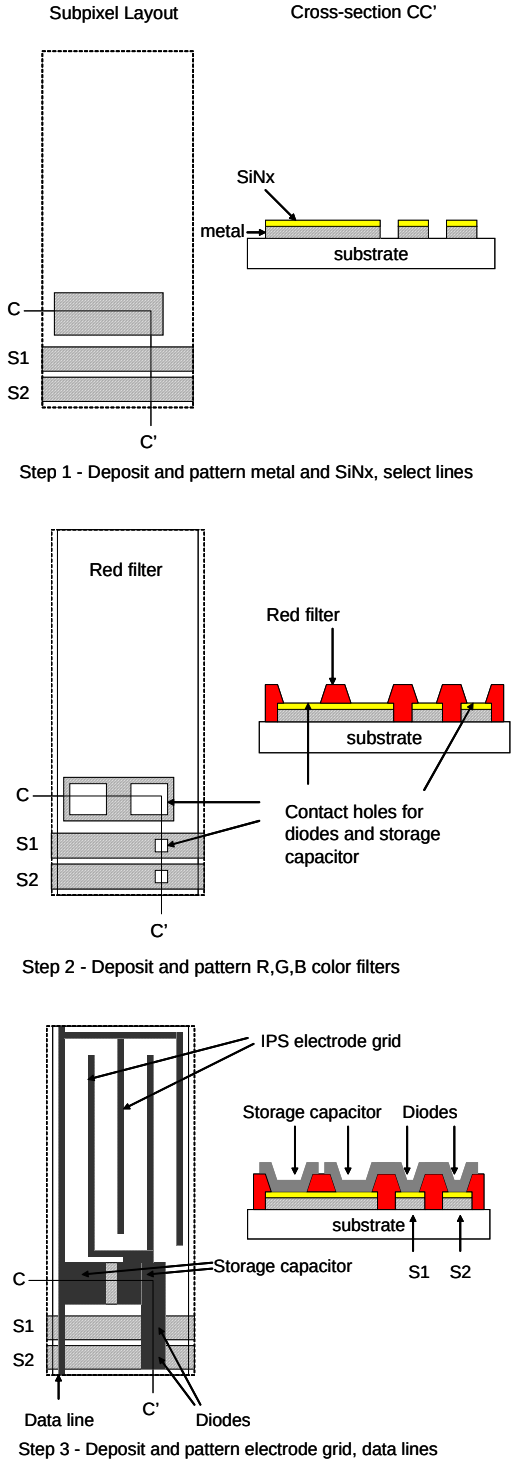

Figure 5. Process sequence and pixel layout for proposed DSD IPS LCD

The color filters are the insulation dielectric between the select lines and data lines. Their thickness and low dielectric constant assist keeping RC delays on the buslines low. The total number of masks for the active substrate and counter substrate combined is only five (or six when a black matrix is added). This compares favorably with the total combined number of mask steps of nine or ten in a standard TFT LCD.

The area of the diodes is designed to be much smaller than the area of the storage capacitor, so that the equivalent circuit can be represented as shown in figure 6. When a select pulse is applied across the series connection of diode and storage capacitor, most of the voltage will appear across the diode and only a fraction across the storage capacitor (as a result of the capacitance division effect). At low voltage the SiNx insulator does not conduct and is sufficiently retaining charge on the storage capacitor, as illustrated in figure 7.

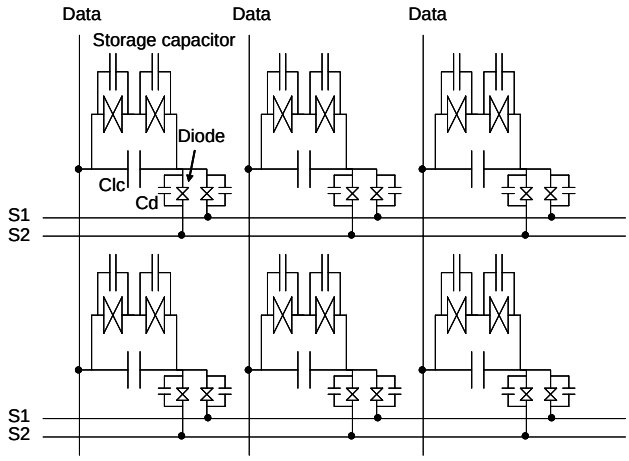

Figure 6. Equivalent circuit of six pixels in DSD IPS mode LCD with storage capacitors much larger than the diodes

In this type of process the SiNx diode area is determined by the contact hole area in the color filter. The SiNx layer underneath extends over the select line. The top electrode of the diode does not make a step over the edge of the bottom electrode (as in a conventional cross-over diode). In conventional cross-over diodes the step at the bottom electrode edge is a weak point and can lead to early breakdown of the diode. The diode reliability is therefore expected to be improved with the elimination of the step in the contact hole configuration of figure 5.

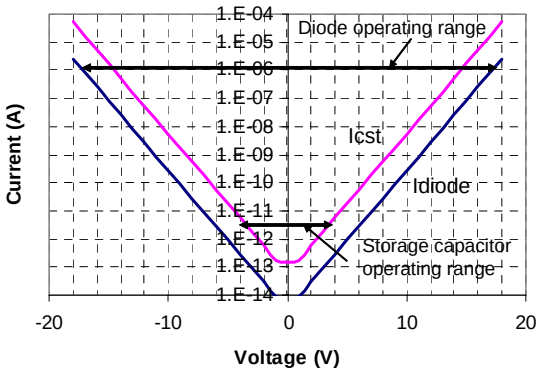

Figure 7. Operating voltage range for the SiNx diodes and the SiNx storage capacitor

4. Summary

Two novel designs for DSD AMLCDs are proposed to further simplify design or process and reduce cost. The first improvement reduces interconnect and raises aperture ratio by the use of shared select lines between pixel rows. It is of particular interest for smaller LCDs in portable applications.

The second approach improves viewing angle and reduces process steps by using the IPS mode with color filter on array. It has the following advantages:

- Improved viewing angle as compared to conventional TN mode
- Minimized total combined mask count and process steps for the active array substrate and the top substrate of the LCD
- Added storage capacitance at each pixel to optimize gray scale control
- Elimination of all patterning steps on the top substrate, so that there is no critical alignment between the two substrates in large area manufacturing (on e.g. ~2 m x 2 m substrates)
- Minimized RC delays on the buslines so as to maximize the possible size of the DSD LCD

This second approach offers a lower cost process for larger displays such as LCD TVs.

7. References

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[11] US Patents #5,926,236 and 6,008,872

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