A Roll-to-Roll Process for Manufacturing Flexible Active-Matrix Backplanes Using Self-Aligned Imprint Lithography and Plasma Processing

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Abstract

Inexpensive large area arrays of thin film transistors (TFTs) on flexible substrates will enable many new display products that cannot be cost effectively manufactured by conventional means. This paper presents a new approach for low cost manufacturing of electronic devices using roll-to-roll (R2R) processes exclusively. It was developed in partnership by Hewlett Packard Laboratories and Iowa Thin Film Technologies (ITFT), a solar cell manufacturer. The approach combines ITFT's unique processes for vacuum deposition and etching of semiconductors, dielectrics and metals on continuous plastic webs with a method HP has invented for the patterning and aligning the multiple layers of a TFT with sub-micron accuracy and feature size.

1. Introduction

Compared to conventional batch fabrication, R2R fabrication of electronic devices on continuous plastic webs offers the possibility of greatly diminished cost. The reasons for the lower expected cost of R2R manufacturing are:

- lower substrate cost
- continuous steady-state processes eliminate the transients and latency in batch processing, thereby increasing throughput, and consistency
- rolled up web provides barrier to particulate contamination reducing clean room requirements
- superior scaling of equipment and process

Technical challenges and a well-entrenched batch fabrication infrastructure have stymied the transition to R2R manufacturing despite its potential advantages. New roll-based tools for the deposition and etching need to be developed. Plastic substrates impose a lower process temperature ceiling making it more difficult to obtain high performance TFTs. However the critical technical challenge for R2R is the capability to pattern and align micron scale features on a large dimensionally unstable substrate.

ITFT has 15 years of experience as the world's only manufacturer of solar cells on plastic substrates with a R2R process. They have developed tools for vacuum deposition and anisotropic etching of metals dielectrics and semiconductors on 1/3 meter wide webs.

A R2R based self aligned imprint lithography (SAIL) process, conceived by HP provides an innovative solution to the patterning and registration of device features on flexible substrates. The SAIL technique is to integrate all the pattern and alignment information for the complete device fabrication into a single 3D mask that is imprinted on the substrate. Since this monolithic masking structure distorts with the substrate, alignments are preserved throughout subsequent processing. A series of etches are applied to the 3D mask to reveal the patterns for each level.

2. R2R Plasma Processing

Many researchers are attempting to force the migration of conventional wafer-based batch processing tools and techniques to large area flexible substrates. We started with the premise of a R2R manufacturing environment and have invented processes for fabrication of thin-film electronics that are explicitly designed for the unique requirements of R2R manufacturing. In our process all of the deposition steps are performed prior to any patterning. This approach is well suited to an inline sequential R2R deposition system. Inline deposition of the full TFT stack avoids contamination of critical interfaces, minimizes the footprint of the deposition equipment, and relaxes clean room requirements for subsequent processes. The process technology and equipment that ITFT has developed for the low temperature PECVD deposition of amorphous silicon solar cells on plastic

substrates are readily extensible to the deposition of the TFT stacks required for active matrix backplanes. Figure 1 shows ITFT's amorphous silicon solar cells produced on 50 µ polyimide webs.

Figure 1. Amorphous Silicon Solar Cell on Plastic Substrate

3. Self-Aligned Imprint Lithography

HP has invented a method for patterning and aligning the multiple layers of an electronic device with micron scale accuracy and feature size over large areas using imprint lithography. Imprint lithography differs from photolithography in that instead of exposing a photo-masking material optically the pattern is transferred to the masking material by molding it with a compliant stamp. The compliance of the stamp allows sub-micron features to be embossed on a large web having poorly controlled thickness and flatness. A second important difference is that in photolithography after exposing and developing the mask it is either entirely removed from the substrate or it remains at the uniform thickness with which it was initially applied resulting in a 'binary' or 'two-state' mask. In imprint lithography the mask can be imprinted with any shape that can be mechanically released from the mold. In particular the imprinted mask may cover the substrate with regions of various discrete thicknesses creating a 'multi-state' mask as shown in Figure 2. This property forms the basis for HP's invention.

In essence the SAIL process combines multiple binary masking steps into a single 3-D structure that is molded on top of the web after all of metal, dielectric and semiconducting thin film layers that are required for the TFT array have been deposited on it. Figure 2 shows the four levels of the imprinted stamp in the vicinity of the TFT channel. After the molding step, subsequent etching steps are used to complete the device. Since all of the patterning information is transferred in the imprinting step any distortion of the web due to subsequent processing will not affect the critical alignments between layers such as the gate-channel alignment.

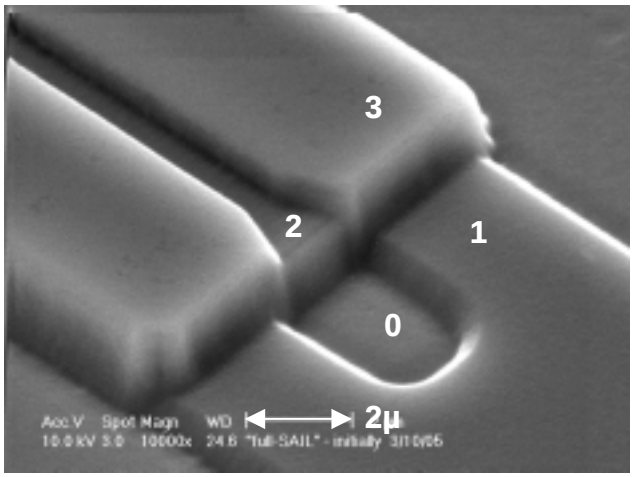

Figure 2. Multilayer Imprinted Mask R2R Imprinted on TFT Stack

HP has made a prototype R2R imprinting machine pictured on Figure 3. Starting from the supply roll the web first passes through a gravure coater where a UV curable photopolymer is applied dilute in solvent. The coated web then passes between the nip of the imprinting roller and a backing roller. The imprinting roller is a quartz cylinder around which a transparent elastomeric stamp is wrapped. The elastomeric stamp contains the 3-dimensional geometry that will be transferred to the coated web. When the web passes

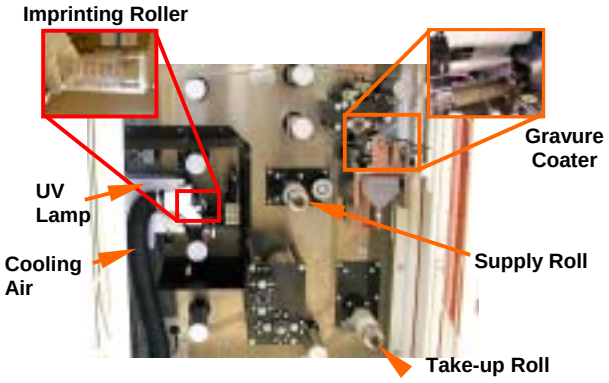

Figure 3. Prototype Imprinting Machine

between the imprinting roller and the backing roller the photopolymer fills the voids in the elastomeric stamp. At this point it is exposed to UV light and is cured. As the coated web exits the nip it is released from the elastomeric stamp and spooled onto the take-up roller. We have demonstrated the imprinting of 40nm features with this method. The have demonstrated a throughput of 5 m/min with the prototype which is limited by the speed of the web transport motors.

4. Initial Device Measurements

As an initial demonstration of the R2R materials development bottom gate TFT test structures were fabricated using R2R deposited bottom metal and dielectric layers. The remaining layers of the device were deposited with shadow masks after the web was singulated.

First, using R2R processes, the 50 µ thick polyimide web was sputter coated with aluminum followed by PECVD deposition of a 375 nm thick silicon oxynitride layer at 275 °C. The web was then singulated into 100 mm X 100 mm squares for subsequent processing. Zinc tin oxide (ZTO), 50 nm thick was sputtered deposited from a $ZnO:Sn_2O$ 1:1 target through a shadow mask to define the active layer of the transistor. The substrate was held at room temperature during the ZTO deposition and then was increased to 250 °C for 10 minutes. Then source and drain electrodes were deposited through a second shadow mask, first using ITO to form a low contact resistance *n*+ contact followed by Al or Au to form the top contacts and contact pads. The channel length was 80 µ defined by the source and drain electrodes and the channel width, defined by the width of the ZTO was 1000 µ. Figure 4 Shows the output characteristics of the transistor. The on-off ratio for this device was greater than 10^6 and the field effect mobility calculated from the linear portion of the transfer characteristics was 15 $cm^2/V/S$.

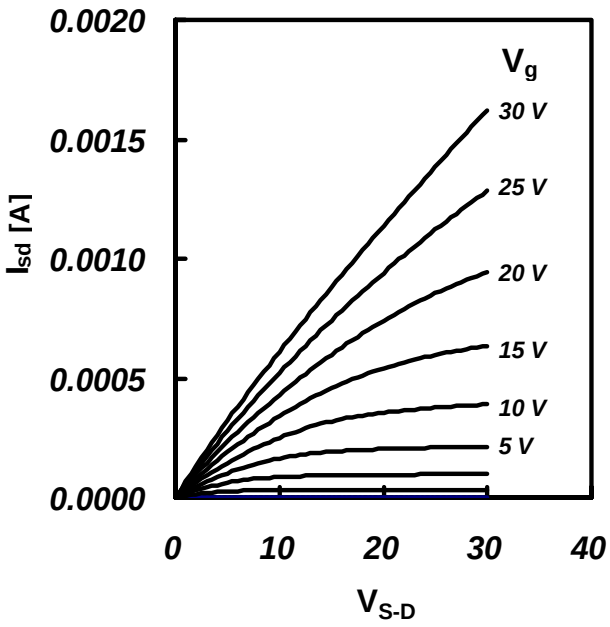

Figure 4 Output characteristics for a bottom gate ZTO transistor with ITO contacts

5. Acknowledgements

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