Rear-Projection CRT Deflection Circuit System

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Abstract

Discussion of this study is that a horizontal deflection system satisfactory of operating at horizontal scan rates from 30KHz to 50KHz has been developed. It will be used in the large-area, color, high-resolution and multi-sync rear-projection CRT display device. Its characters, including the description, analysis and deflection circuit loss, are presented.

Keywords:

Projection, CRT, Deflection, multi-sync, loss

Introduction

The projection CRT (cathode ray tube) technologies are based on relatively mature electron beam scanning techniques. Compared with the micro-display devices, projection CRT technology dominates the electronic projection display's market at the present [1].

A high performance horizontal deflection system requires satisfying the range of possible HDTV video sources. There are also existing display devices operating at fixed scan rates, e.g. Sony's DDM 2801 [2]. In 1992, A multi-standard digital convergence and focus system has been developed for both rear and front projection TV, demonstrating high picture quality and different picture zoom modes [3].

As video recorders and video displayers have become popular, the users of video products for entertainment require more beautiful and powerful large screen pictures for a home theater.

The objective of this work is to present the design solutions in the development of the variable frequency horizontal deflection system and the deflection circuit loss of this deflection system.

Horizontal Deflection Desctiption

A basic deflection circuit is shown in Fig. 1. Its equivalent circuit is shown in Fig. 2.
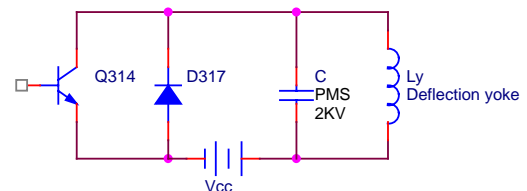
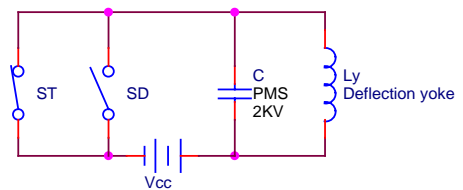

Fig. 1 Basic Horizontal Deflection Circuit

Fig. 2 Equivalent Horizontal Deflection Circuit

The operation waveform of Fig. 2 is shown in Fig. 3. Fig. 3(a) is the base input voltage waveform of Q314. Fig. 3(b) is the current waveform of ST. Fig. 3(c) is the current waveform of SD. Fig. 3(d) is the current waveform (I_{Ly}) of Ly (Ly is deflection yoke). Fig. 3(e) is the voltage waveform of ST. The operation steps are discussed as follows: (1)

t1~t2: ST close, SD open, and the current of Ly is increasing. (2) t2~t3: ST open, SD open, and C is charged by the storage current of Ly. The voltage of ST will rise to the peak value (V_{CP}). (3) t3~t4: ST open, SD open, and C will discharge its storage current and charge for Ly. (4) t4~t5: ST open, SD close, and Ly will discharge its storage current to zero.
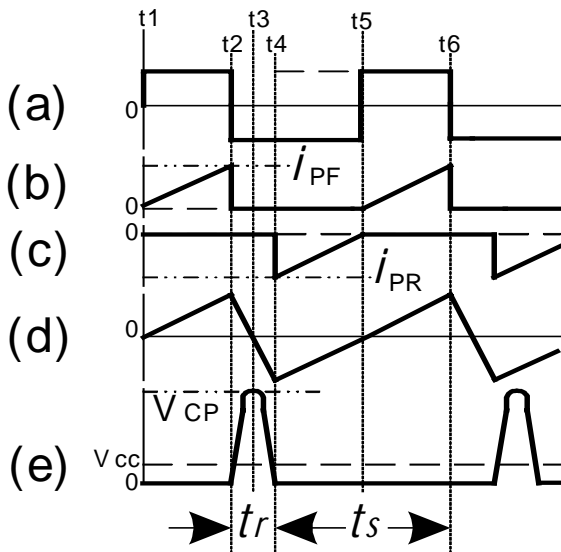

Fig. 3 Operation Waveforms of Basic Horizontal Deflection Circuit

The forward peak current of ST (i_{PF}) is: $i_{PF} = \frac{V_{CC}}{2L_y} t_s$. The peak voltage of ST (V_{CP}) can be expressed as: $V_{CP} = 2\pi f_r L_y i_{PF} + V_{CC}$, where $f_r = \frac{1}{2\pi\sqrt{L_y C}}$. The backward current of ST (i_{PR}) is equal to i_{PF}. The current of Ly is assigned to be i_{PP}, where $i_{PP} = i_{PF} + i_{PR}$. The retrace time is t_r , $t_r = \frac{1}{2f_r}$. More specifically, $t_s = t_H - t_r$, t_H is total horizontal deflection period. The equation for peak voltage (V_{CP}) can be written as

$$V_{CP} = V_{CC}\left[\frac{\pi}{2}\left(\frac{t_H}{t_r} - 1\right) + 1\right]. \tag{a1}$$

The development of the variable frequency horizontal deflection system accommodates diverse video timings by adjusting the width and the retrace time [4].

Deflection Circuit Power Lose

There several kinds of deflection circuit power losses are discussed as below. In scan stage, the deflection circuit power lose includes the deflection yoke impendence lose and the transistor internal impendence lose. The deflection yoke impendence lose:

$$P_y = R_y \cdot \left(i_{PP} / 2\sqrt{3}\right)^2 \cdot \frac{t_s}{t_H} = \frac{R_y i_{PP}^2}{12} \cdot \frac{t_s}{t_H}$$

$$= \frac{1}{12} \cdot \frac{R_y}{L_y} \cdot \frac{t_s}{t_H}\left(L_y i_{PP}^2\right). \tag{a2}$$

The transistor internal impendence lose is:

$$P_s = r_s \cdot \left(i_{PP} / 2\sqrt{3}\right)^2 \cdot \frac{t_s}{t_H}$$

$$= \frac{1}{12} \cdot \frac{r_s}{L_y} \cdot \frac{t_s}{t_H}\left(L_y i_{PP}^2\right). \tag{a3}$$

In blanking stage, the deflection circuit power lose includes the resonance lose and the falling time lose. The falling time is called cut-off time (t_{C0}) of the transistor. The falling time power lose of the transistor is

$$P_{C0}, \quad P_{C0} \approx \frac{\pi^2}{96} \cdot \frac{L_y i_{PP}^2}{t_H} \cdot \left(\frac{t_{C0}}{t_r}\right)^2. \tag{a4}$$

The resonance loss in blanking stage is P_r,

$$P_r = P_d\left(1 - e^{-\pi/Q}\right), \tag{a5}$$

Where $Q = 2\pi f_r L_y / R_y$,

$$P_d = \frac{1}{2}L_y i_{PF}^2 f_H = \frac{1}{2}\frac{L_y i_{PP}^2}{\left(1 + e^{-\pi/2Q}\right)^2} \cdot f_H \text{, and}$$

f_H is horizontal deflection frequency [4].

Multi-Sync Deflection System Architecture

Fig. 4 shows the block diagram of the multi-sync horizontal deflection system. It is a resonant fly-back system producing a linear scan. The pattern generator provides variable RGB video signals and variable horizontal/ vertical syncs. The necessary analog control signals are obtained from microcontroller via an IIC digital interface. A dynamic B+ voltage (B+ voltage is the generally appellation as

mentioned V_{CC} in Fig. 2.) is provided by modulator of the DC-to-DC circuit controlling the width of the scan. The deflection signal control circuit provides synchronization processing, horizontal and vertical synchronization with full auto-sync capability and very short settling times after mode changes [5]. The vertical output circuit is a vertical deflection booster. The horizontal output circuit is a standard horizontal deflection booster circuit. Different horizontal scan frequency generated by pattern generator will produce varied retrace time, and so the DC-to-DC circuit must be designed to maintaining the constant anode high voltage. The high voltage generator can produce and stabilize the anode high voltage. The video pre-amp is used to amplify the RGB video source, and the PCRT (Projection CRT) Driver is used to driving the projection picture tube.
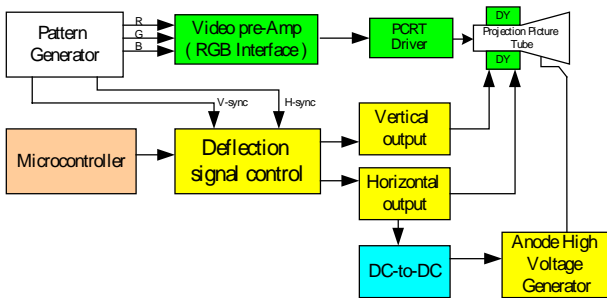

Fig. 4 Multi-sync deflection system block diagram

Multi-Sync Deflection Circuit Design and Experimental Result

Fig. 5 shows details of multi-sync deflection circuit design. The horizontal output circuit employs a dedicated power switch 1700V MOSFET driver IC, which part number is 2SC5588. This IC is still showing in Fig. 1 and Fig. 5, which reference number is Q314. The pincushion and keystone compensation is implemented by modulating the B+ voltage. The S-correction is provided by appropriate capacitors for controlling the yoke current. The three yokes (for red, green and blue sources) are paralleled and driven together by a power switch 1700V MOSFET driver IC. The

regulator of the DC-to-DC circuit is a boost converter operating from 30kHz to 50kHz. A photo of the horizontal deflection board, three projection picture tubes and their driver board are shown in Fig. 6. The experiment result of multi-sync deflection circuit is shown in Fig. 7. The designed multi-sync deflection circuit is tested from horizontal scan frequency 31kHz to 48kHz. Fig. 7 shows the current waveforms (I_{Ly}) of deflection yoke current and the voltage waveforms (V_{CP}) of power switch MOSFET driver IC.
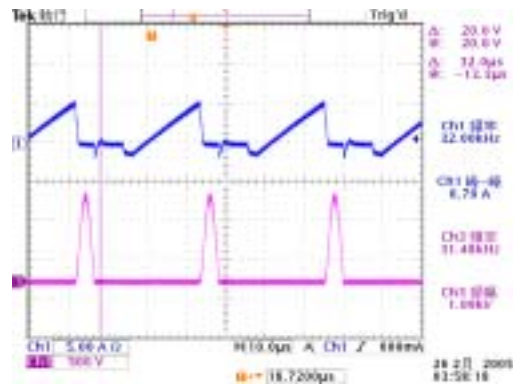

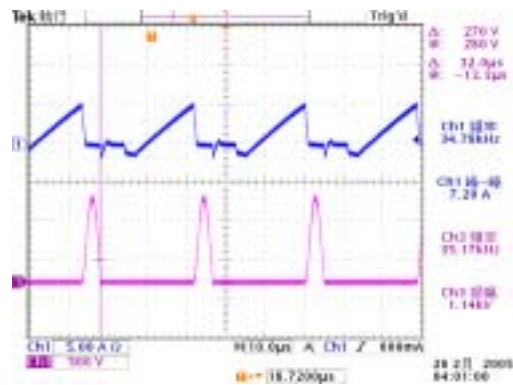Fig. 7(a) Horizontal scan frequency: 31.5kHz
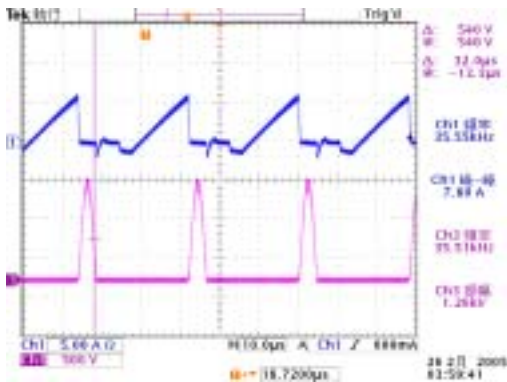

Fig. 7(b) Horizontal scan frequency: 35kHz

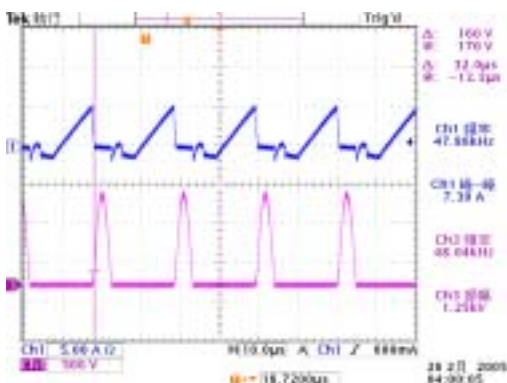Fig. 7(b) Horizontal scan frequency: 36kHz

Fig. 7(b) Horizontal scan frequency: 48kHz

Conclusions

In this paper, the multi-sync horizontal deflection system using in rear projection cathode ray tube device is introduced. This device is different from the fixed scan frequency horizontal deflection system. The advantage of the multi-sync horizontal deflection system includes the superior picture quality, low circuit power loses and more video sources compatible. This multi-sync horizontal deflection system incorporates four different retrace times (31kHz, 35kHz, 36kHz, 48kHz), and its resolution can rise to HDTV @1080i spec.

References

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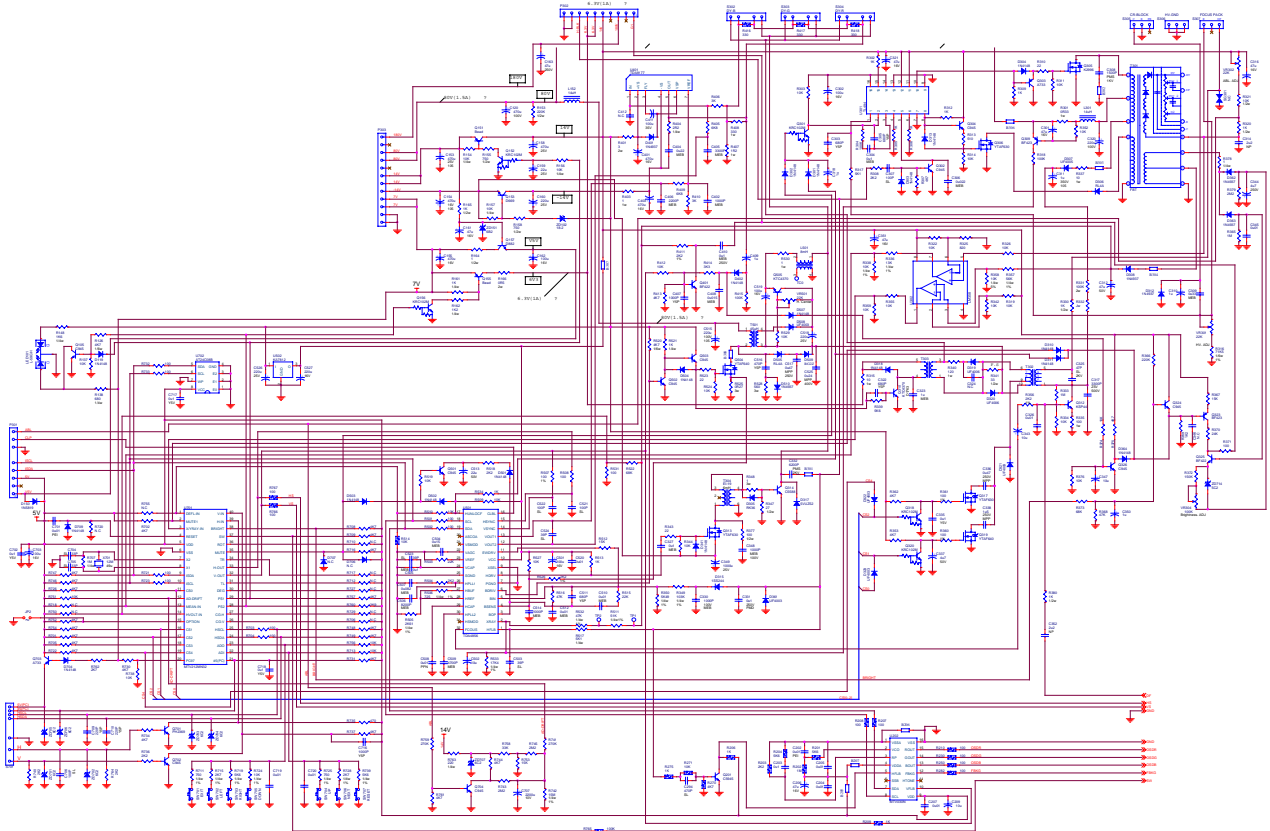*Fig. 6 Photograph of the horizontal deflection board, three projection picture tubes and their driver board.*

Fig. 5 Circuit diagram of multi-sync horizontal deflection circuit design