# Poly-Silicon TFT's on Metal Foil Substrates for Flexible Displays

*Miltiadis Hatalis, M. Troccoli, T. Chuang, A. Jamshidi, G. Reed*
**Department of Electrical Engineering, Lehigh University**

## Abstract

*In an attempt to fabricate all inclusive display systems we are presenting a study on several elements that would be used as building blocks for all-on-board integrated applications on stainless steel foils. These systems would include in the same substrate all or many of the components needed to drive a flat panel OLED display. We are reporting results on both digital and analog circuits on stainless steel foils. Shift registers running at speeds greater than 1.0MHz are shown as well as oscillators operating at over 40 MHz. Pixel circuits for driving organic light emitting diodes are presented. The device technology of choice is that based on poly-silicon TFT technology as it has the potential of producing circuits with good performance and considerable cost savings over the established processes on quartz or glass substrates (amorphous Silicon a-Si:H or silicon on Insulator SOI).*

## 1. Introduction

During the past decade, there has been an increased focus on the development of highly integrated large area electronics on flexible substrates. The main application targeted is displays and other matrix-based electronics on a systems-based approach. The appeal of flexible electronics rests in their ability to realize novel circuits whose space and mechanical restrictions do not permit the use of a rigid substrates or printed circuit board. Furthermore, they could potentially be fabricated with a roll-to-roll manufacturing process similar to a rolling photolithographic printing process, which can produce this type of circuits with a throughput many times higher than normal semiconductor processing.

Displays are one of the preferred flexible electronic applications because of the mechanical and space saving advantages a conformal or foldable display would have (robust, lightweight). Display active panels have relatively relaxed requirements for pixel electronics devices such as thin film transistor (TFT) switches and current sources. However, a larger degree of system integration requires the incorporation of high performance digital and analog circuits for display driving and signal processing. A higher integration level is desirable, because it is shown to increase system yield by reducing external connections (which are a substantial source of failure) and substantially decreasing manufacturing costs.

The fabrication of highly integrated large area systems on flexible substrates with reasonable performance characteristics is - at this time - possible only with polysilicon. The high carrier mobility values that can be obtained with this approach, and the prospect of realizing highly efficient, low power CMOS circuitry are the two strongest assets of polysilicon TFT technology.

On this paper, we are presenting high-speed polycrystalline silicon thin film transistor digital circuits as well as all the elements needed for the fabrication of a display, representing some of the building blocks for such integrated systems. Both n-channel and p-channel excimer laser re-crystallized poly-silicon devices with effective mobility values in the region of 250cm2/Vs and 100cm2/Vs respectively, and ON vs. OFF current ratios at least seven orders of magnitude have been fabricated, and their characteristics are presented. Ring oscillators running at frequencies above 40MHz are described, along with static and dynamic shift registers, with maximum clock frequency exceeding 1.0MHz. The presented results indicate the potential of these circuits for possible row and column driving for displays or memory addressing.

## 2. Circuit Fabrication

Type-304 Stainless steel foils, 100μm thick, were manually and chemically polished and cut to 100mm diameter wafer size substrates. The manual and chemical polishing step was developed and used in order to reduce the surface roughness of the untreated foils, which approached 1500Å. After polishing, an RMS value of surface roughness approaching 100Å was obtained.

After cleaning, the substrates were coated with an isolation layer of PECVD $SiO_2$, 750nm thick. The active amorphous Si film was PECVD deposited, crystallized with an Excimer Laser and patterned to form the TFT islands, 1000Å thick. The gate dielectric was PECVD silicon dioxide 1000Å thick,

followed by a PECVD a-Si layer for the gate electrode. After these depositions, the gate electrode was n+ ion implanted and patterned, followed by the patterning of the gate dielectric and the drain / source region formation through p+ ($BF_2$) or n+ (P) ion implantation.

The drain and source TFT regions and poly-Si inter-connects were silicided using sputtered Ni and an in situ anneal at 400°C. A passivation oxide layer 3000Å thick was PECVD deposited and followed by the patterning of contact holes. In order to avoid aluminum hillocks that can lead to circuit failure, AlNi was selected as the most suitable metalization layer for this purpose. Aluminum and nickel were sputtered to a total thickness of 3000Å, then annealed in situ to form the alloy. After patterning the metal, the devices and circuits were measured.

## 3. Circuit Performance

Stand alone devices of various geometries were fabricated and tested, and their electrical characteristics are presented below. The minimum fabricated channel length was 2μm (minimum feature size). Figure 1 shows the $I_{DS}/V_{GS}$ characteristics of two devices, taken at $|V_{DS}|$ = 0.1V and 1.1V. Stand alone p- and n-type devices were measured, and their basic characteristics were recorded. Table 1 shows the average values of mobility, threshold voltage, inverse sub-threshold slope and off current for both types of gate oxide TFTs. For all devices, there is a difference between Id(ON) and Id(OFF) at least six orders of magnitude, which is one of the highest compared with previously published results.

| Device (W/L=20/4) | Mty. (cm^2/Vs) | Vt (V) | SS (V/dec) | Ioff (A) |
|---|---|---|---|---|
| NMOS | 200 | +1.4 | 1.4 | 1 pA |
| PMOS | 87 | -9.8 | 2.4 | 0.1 pA |

**Table 1**: Average values of PMOS and NMOS TFTs

A basic circuit for the evaluation of digital circuit performance is a ring oscillator (RO). The oscillators we have fabricated are composed of 19 CMOS inverter stages, and have buffered outputs. Both NMOS and PMOS devices have the same geometry 20μm/4μm. Powered with a supply voltage of 15V, its free running frequency was measured to be approximately 40.4MHz. This results in an average delay time of 1.302ns per inverter stage.

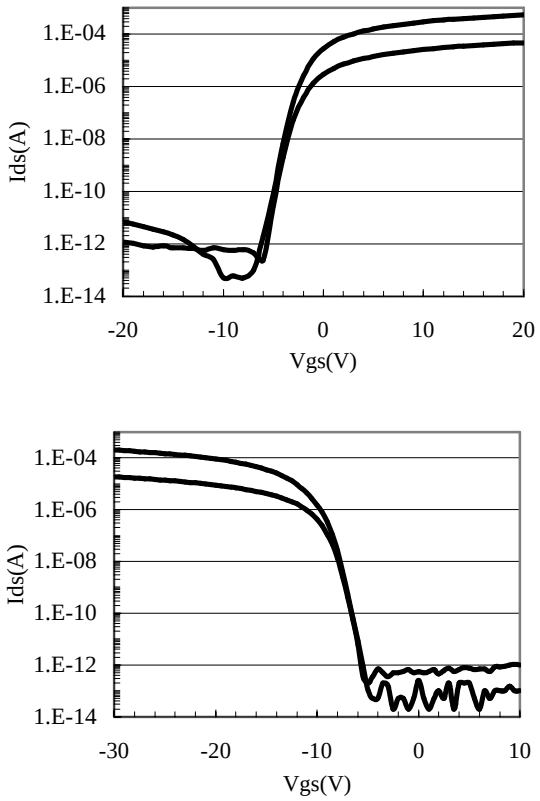


**Fig. 1:** Typical characteristics of PECVD oxide NMOS and PMOS devices at Vds=0.iV and 1.1V (W/L=20/4)

One of the most important memory and display driver circuits (for both active- and passive-matrix displays) is a shift register. Assuming the simplest driving scheme, the rows and the columns of the display matrix are activated one at a time, which is accomplished by the active shift register output (which can be high or a low signal) being shifted to the next bit, and eventually cycled to the register's input again.

Two types of shift registers have been designed and evaluated: a static, D-type latch-based design and a dynamic pass-gate gate design. Both are 10-bit, serial input, parallel output designs. Both are based on the clocked CMOS ($C^2MOS$) logic architecture, which uses a non-overlapping pseudo two-phase clock signal for shift timing. The circuit schematics are shown in Figure 2; labels indicate the W/L ratios of the TFTs.

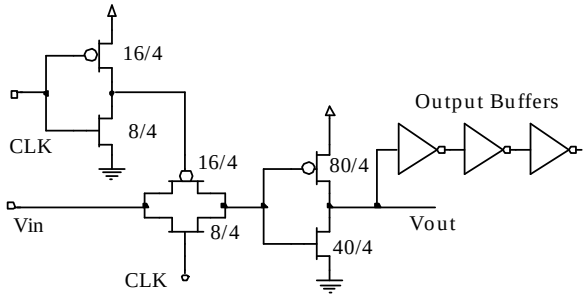


**Fig. 2:** One-half bit stage schematics of the fabricated dynamic

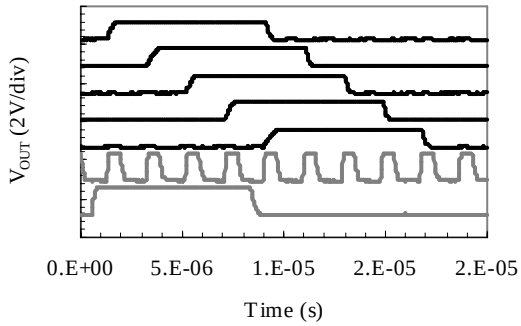


**Fig. 3**: Output waveforms of dynamic shift registers, at 500 kHz

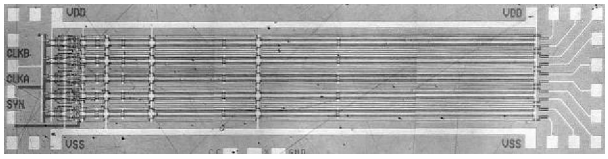

**Fig. 4:** Dynamic 10-stage shift registers on stainless steel foil.

## 4. Pixel Architectures

Two different circuit architectures have been implemented. The first one is the standard 2- TFT design. In this circuit, M1 behaves as a voltage controlled current source, and M2 is the control switch. This means that there are three lines going into each pixel (Vdata, Vadd and Vdd). This circuit works as follows: an analog voltage is programmed in the data line during addressing time (when M2 is turned ON by the address line.) This voltage activates M1 allowing a controlled current to flow through it. When the addressing period is over, M2 is turned OFF and C stores the data voltage. This allows M1 to keep supplying the correct current during the non-addressing time. This pixel architecture was implemented with two topologies: an all PMOS design, and a CMOS design with the driving transistor being NMOS and the switch being PMOS.

This circuit does not compensate for TFT device parameter variations such as mobility or threshold voltage. Several pixel designs have been proposed to compensate for such variations. One approach that has attracted a great deal of interest in the last few years is the current addressing technique. When directly addressing with a current, turn-ON voltages and mobility variations do not affect the LED current. This is done by programming the current source with a reference current instead of a voltage, so the current provided by that source is not a function of the voltage on the transistor's gate (instead, the voltage on the gate is a function of the current.)

The 4 TFT current copy circuit is perhaps a good compromise between performance and complexity. This circuit works as follows: during addressing time, a reference current is sinked through Idata. Since M1 is diode connected, a corresponding voltage is established on its gate to allow that current to flow. When M2 and M3 are turned OFF and M4 is turned ON, C holds the programmed voltage on the gate of M1 allowing that current to now flow through the diode. (Figure 5 shows both pixel architectures)

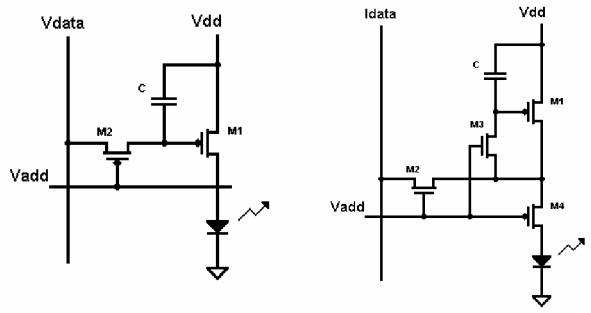


**Fig. 5:** 2 TFT PMOS pixel (left) 4 TFT pixel (right).

Both architectures were implemented with two different layouts. The more traditional layout requires a power supply line. However, when using metal foil substrates the high conductivity of stainless steel can be used to bring in power to each pixel creating a less resistive power distribution. The main motive for developing this approach was to increase the light emitting area of the display, since the common power supply line can be omitted. An extra contact layer is required to create contacts between the pixels and the substrate. These contacts are formed after the patterning the first metal contact holes during the fabrication of electric circuits. A second PECVD passivation oxide follows, and then vias that make

contact between the AlNi layer and the Indium Tin Oxide film that follows are patterned and opened. After the patterning of the ITO film, the organic electroluminescent material is deposited, followed by the OLED cathode deposition and final display encapsulation.

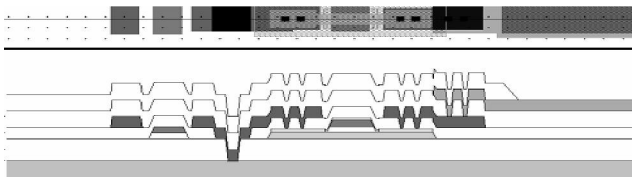

**Fig. 6:** The AM-OLED pixel structure on steel and cross section (vertical dimensions not to scale)

## 4. Pixel Performance

The overall functionality of both pixel designs and both layout implementations were proven at different load impedances 10K, 50K and 100K to account for possible variations in OLED performances. Also the 2-TFT pixel was demonstrated with three pitch sizes: 250 x 250 um and 110 x 105 um for the PMOS implementation, and 125 x 125 um for the CMOS implementation.

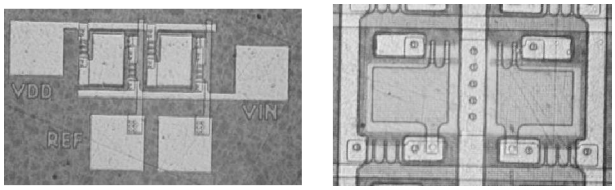


**Fig. 7:** 2 TFT pixels 125 um x 125 um (left) and 2 TFT pixels 110um x 105 um (right)

Figure 8 shows the average current measured through different pixels over a range of data values and its normalized variation as a function of data voltage, in the 2 TFT pixels. This normalized variation curve was extrapolated to obtain percentage variation of threshold voltage and mobility of the measured devices. We can obtain the theoretical variation by solving the difference equations for mobility (1) and threshold voltage (2) at different gate bias. (First level approximation done with TFT's working on saturation.)

$$\partial I = \partial\mu \cdot k \cdot (Vgs - Vt)^2 \quad (1)$$

$$\partial I = \partial Vt \cdot 2 \cdot k \cdot \mu \cdot (Vgs - Vt) \quad (2)$$

If we normalize for the absolute value of current and notice that $\partial\mu = \overline{\mu} \cdot \xi_{\mu}$ and $\partial Vt = \overline{Vt} \cdot \xi_{Vt}$ (where $\overline{\mu}$, $\xi_{\mu}$ and $\overline{Vt}$, $\xi_{Vt}$ are the average and the percentage mobility and threshold voltage variations respectively), we obtain:

$$\frac{\partial I}{I} = \xi_{\mu} \quad (3)$$

for mobility changes of $\xi_{\mu}$ percent , and

$$\frac{\partial I}{I} = 2 \cdot \frac{\overline{Vt} \cdot \xi_{Vt}}{Vgs - \overline{Vt}} \quad (4)$$

for threshold voltage changes of $\xi_{Vt}$ percent.

The extrapolated numbers from figure 9 were 4% for mobility and 9% for threshold voltage which approximate the actual variations seen when obtaining Table 1.

Figure 9 shows the output current versus the programming current in the 4 TFT pixels. The nonlinearity at low current levels can be explained by assuming non-saturation behavior of the driving TFT's. Furthermore, the line impedance that the driving TFT sees when programming is different from the OLED's impedance. As a consequence, the finite output impedance for these devices also explains the loss of linearity between programming current and operating current.

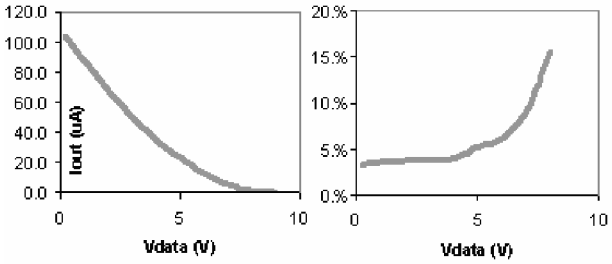


**Fig. 8:** Typical output current versus input data for 2 TFT pixels and normalized deviations

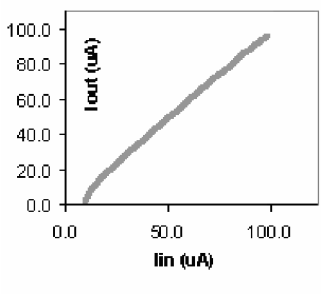


**Fig. 9:** Output current vs. programming current in 4 TFT pixel

## 5. Conclusion

This paper discussed fabrication and performance results of excimer laser annealed poly-silicon TFT devices, circuits and display elements on flexible, type-304 stainless steel foil substrates. We have demonstrated this is possible with a high temperature, CMOS compatible poly-Si TFT fabrication process. This process has resulted in devices adequate not only for active matrix displays implementations, but for integrated display driver circuits too, further enhancing the cost savings realizable with this approach. The functionality of several pixels has been proven and stand alone PLED structures have been demonstrated on stainless steel substrates.

These results justify the fabrication of high performance digital circuits for display driver and other medium to high-speed applications on flexible metal foils, and underscore the substantial practical advantages of this type of substrate for high volume, low cost highly integrated flexible electronics.

## 6. References

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