New Charge-Recycling Structure and Driving Scheme for TFT-LCD Source-Driver IC Application

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Abstract

New charge-recycling structure and driving scheme for TFT-LCD source-driver IC application are proposed. The number of additional switches for the charge recycling is greatly reduced. An experimental prototype 6-bit source driver with five-level seven-phase charge recycling implemented in a 0.35-μm CMOS technology demonstrates that the quiescent current is only 3.1 mA, dynamic power saving is 75 %, and the settling time, which includes the charge-recycling and data driving, is within 25 μs.

1.   Introduction

As color liquid-crystal displays (LCDs) are recently installed in mobile products such as mobile phones, there is a big demand of developing low-power dissipation LCD driver [1-4]. The power dissipation in a typical source driver is composed of three parts. They are: the power dissipation of the digital part, the static power consumption due to the dc bias current to the DAC's and buffer amplifiers, and the dynamic power dissipated in charging capacitive outputs. Since hundreds of buffer amplifiers are built in a single source-driver IC and the buffer amplifiers drive hundreds of highly capacitive column lines with high voltage drive, the dynamic power dissipated in charging the capacitive loads and the dc bias power supplied to the buffer amplifiers are dominated in the source-driver IC.

Some schemes were proposed to reduce the dynamic power dissipation. For examples, Erhart et al. [4] proposed a charge conservation for the dot inversion method. This scheme can reduce the dynamic power by 50%. Kim et al. [5] proposed a multi-level multi-phase charge-recycling method for low-power AMLCD column drivers. The author proposed this charge-recycling method to reduce the power consumption incurred in driving highly capacitive column lines by storing the charge into the external capacitors and reusing it in the next cycle.

Several papers were also proposed and demonstrated to reduce the dc power dissipation. Among them, Lu et al. [1] proposed a rail-to-rail low-power class-B buffer amplifier. Itakura et al. [3] proposed a 402-output TFT-LCD driver IC with power control based on the selection of the number of colors to be displayed. In this architecture, the reference voltage buffers must drive 1-402 capacitive loads. The stability is achieved by introducing a compensation resistor, which is assigned at each output. Although this additional resistor can be used to achieve an enough phase margin, it will increase the charge/discharge time during the charge-recycling period if the same switch network is used for the charge-recycling technique. In this work, we combine the charge-recycling technique and power control scheme to reduce both of the dynamic and dc power dissipation. In order to reduce the number of the switch needed for the charge-recycling technique, the same switch network in the DAC's are used to transfer the charge during the recycling period.

2.   Source-Driver Architecture with Charge-Recycling Technique

A typical charge-recycler is attached between the buffer amplifiers and the column lines. The buffer amplifiers are isolated from the column lines during the charge-recycling period. For this scheme, m x n-switches are needed to transfer the charges on the column lines for an n-output source-driver IC with an m-level charge-recycler [5]. In this work, we use the switches of the DAC's to participate in the charge transference. The number of additional switches is drastically reduced. Figure 1 shows the proposed source-driver architecture with charge-recycling technique. Reference-voltage buffers are located before the DAC's. The switches of DAC's are used to connect the selected reference voltage to the column line during the driving time. However, the same switches are used to transfer the charge between the column lines and the external capacitors.
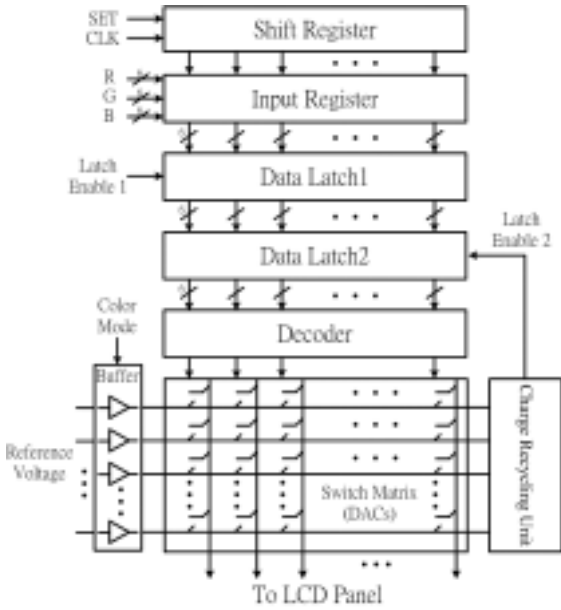
Figure 1 Proposed source-driver architecture with charge-recycling technique.

Figure 2 shows (a) the charge-recycling unit and (b) the corresponding control signals for the 5-level 7-phase charge-recycling operation. The additional switches, SW0 ~ SW4, which are controlled by the charge-recycling controller, are also used to transfer the charge between the column lines and the external charge storage capacitors, C_{ext1} ~ C_{ext5}. The capacitor C_{ext1} is used to store the charges of the column lines with positive polarity and high MSB. However, C_{ext2} is for the column lines with positive polarity but with low MSB. Similarly, C_{ext3} and C_{ext4} are both for the negative polarity but for the high MSB and low MSB, respectively. The capacitor C_{ext5} is for the backside voltage, V_{com}.

Figure 3 shows the concept of the 5-level 7-phase charge-recycling operation. In the first phase, all reference voltage buffers are disabled. Hence all column lines are isolated from the reference voltage sources. In the second phase, all column lines with the same polarity and MSB are connected together to the corresponding external capacitors by turn on the switches SW0, SW1, and SW3. Then the column lines with positive polarity and high MSB are connected to C_{ext1}, but those with positive polarity and low MSB are connected to C_{ext2}. The column lines with negative polarity and high MSB are connected to C_{ext3}, but those with negative polarity and low MSB are connected to C_{ext4}.
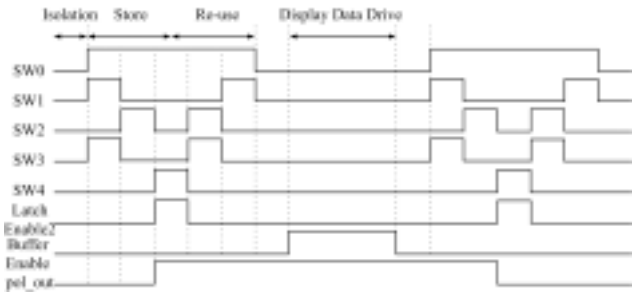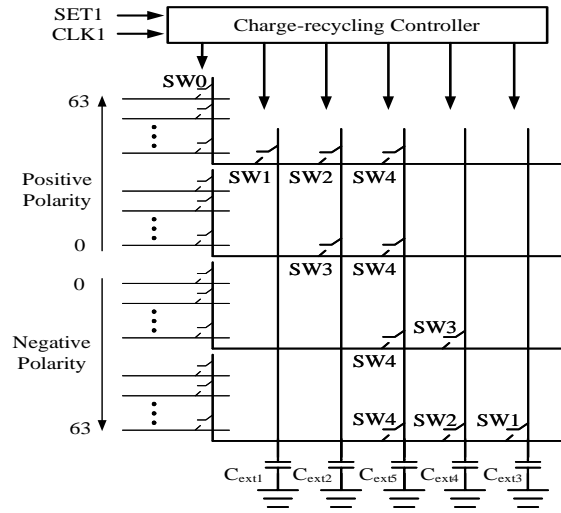

(a)

Figure 2 (a) The charge-recycling unit and (b) the corresponding control signals for the 5-level 7-phase charge-recycling operation.
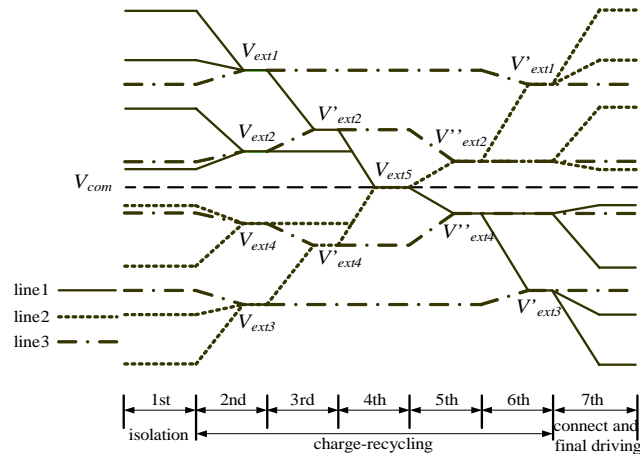

Figure 3 The concept of the 5-level 7-phase charge-recycling operation.

In the third phase, the column lines with positive polarity and high MSB are connected to C_{ext2}, but those with negative polarity and high MSB are connected to C_{ext4} by turning on the switch SW2. In the fourth phase, all column lines are connected to

C_{ext5} and equalized to the backside voltage, V_{com} by turning on SW4. In the fifth phase, the polarity is changed and the next display data are given. All column lines with positive polarity display data are connected to C_{ext2} and those with negative polarity are connected to C_{ext4} by turning SW2 and SW3. The polarities of the column lines are then reversed. In the sixth phase, the column lines with positive polarity and high MSB are connected to C_{ext1}, and those with negative polarity and high MSB are connected to C_{ext3} by turning on SW1. Finally, in the seventh phase, the column lines are connected to their corresponding reference voltage buffer amplifiers and driven to the final voltage levels. Since there is no current drain from the power supply form the first phase to the sixth phase, no power consumption is incurred during these periods. Power is dissipated only in the final phase. The driven voltage is greatly reduced. Hence the power dissipation is greatly reduced. The number of additional switches does not depend on the output number and it is only 138 for a 6-bit resolution 5-level 7-phase charge-recycler for the proposed structure. However, the conventional charge-recycling structure depends on the output number. It needs 2010 additional switches to transfer the charges for a 402-output five-level recycler. The more output and level numbers are the more additional switches are needed.

3. Buffer Amplifiers

Since the buffer amplifiers are located before the DAC's, they must drive the selected column lines through the switches of DAC's. The selected capacitive loads vary in wide range. The number of the loads can range from 0 to the half of the output number. Due to the wide loading condition, the stability should be considered carefully. The phase margin can be achieved by a zero compensation technique, in which a zero is introduced by inserting a resistor between the output of the buffer and the capacitive load. Itakura et al. [3] assigned a resistor in series at each output for one reference voltage buffer. Although this technique can achieve the stability independent of the number of the capacitive loads, the additional resistor in series at each output for one reference voltage buffer will increase the charge-recycling time. Also a number of 128x402 resistors are required for 6-bit 402-output driver IC. In this work, a single resistor is connected directly in series at the output of the reference buffer amplifier. In this way, the compensation resistor will not affect the charge-recycling time and only 128 resistors are

acquired for 6-bit driver IC. Although the settling time increases for a large number of selected capacitive loads, it is reduced by adding a second buffer amplifier. Figure 4 shows the new architecture of reference-voltage buffer, in which an additional class-B buffer amplifier with intentionally built-in offset voltages, A2, is connected to the original buffer, A1 and the compensation resistor, R_Z is connected between the outputs of A1 and A2. The buffer A1 can be either a two-stage class-AB or class-B buffer amplifier. The added buffer A2, which is used to improve the slew rate limiting settling time, is turned off for the vicinity of the stable state.
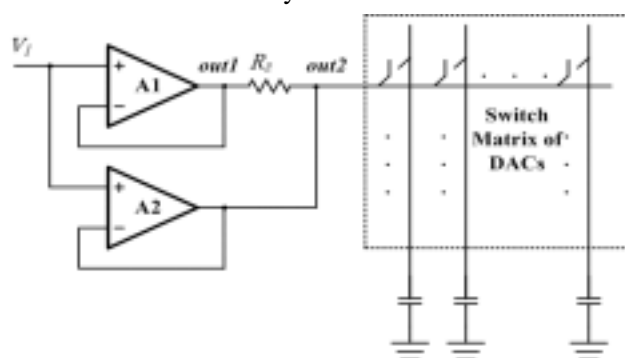

Figure 4 The architecture of reference-voltage buffer.

4. Experimental Results

A 6-bit source driver, which utilized the proposed charge-recycling structure and driving scheme, was fabricated using a 0.35-µm CMOS technology. The photograph of the prototype source driver with 6 channels is shown in Figure 5.
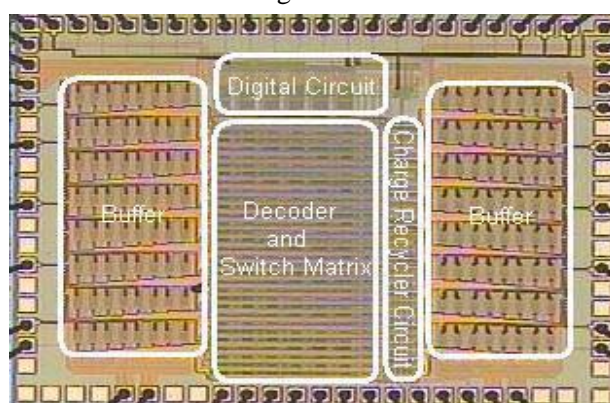

Figure 5 Photograph of the prototype source driver with 6 channels.

Each RGB digital input code is 6-bit wide and the clock frequency is 5 MHz. The proposed source driver is measured under a dot inversion with a power

supply of 3.3 V and a load capacitor of 30 pF for each channel. The measured output waveform of two neighboring channels under dot inversion and five-level seven-phase charge recycling for the RGB digital inputs of '111111' is shown in Figure 6. The settling time, which includes the charge-recycling and data driving, is within 25 μs. The quiescent current is only 3.1 mA. If the output number is extended to several hundreds, the value of quiescent current will not be increased. The experimental results show that the proposed source driver is suitable for VGA and SVGA TFT-LCD applications. The performance summary is shown in Table I.
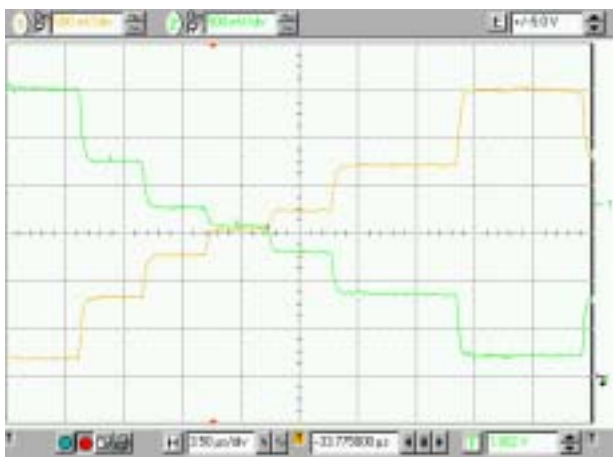

Figure 6 Measured output waveform of two neighboring channels under dot inversion and 5-level 7-phase charge recycling for the RGB digital inputs of '111111'.

Table I Performance Summary

Video signal mode	VGA and SVGA
Supply voltage	3.3 V
Inversion	dot inversion
Pixel clock	5 MHz
Color mode	262144 colors (6 bits)
	512 colors (3 bits)
Load	30 pF
Quiescent current	3.1 mA
Dynamic power saving	75 % (5-level 7-phase charge recycle)
Settling time (Charge-recycling + data driving)	within 25 μs

5. Conclusions

In this work, new charge-recycling structure and driving scheme for VGA and SVGA TFT-LCD source-driver IC applications have been presented. The proposed charge-recycling structure is suitable for the source-driver in which the reference-voltage buffers are located before the DAC's. The number of additional switches for the charge recycle is greatly reduced by using the switches of DAC's to transfer charges between the capacitive column loads and the storage capacitors during the charge-recycling period. A compensation resistor, which will not affect the charge-recycling time, is connected at each output of the reference voltage buffer to achieve the phase margin. An experimental prototype source driver with five-level seven-phase charge recycling implemented in a 0.35-μm CMOS technology demonstrate that the quiescent current is only 3.1 mA, dynamic power saving is 75 %, and the settling time, which includes the charge-recycling and data driving, is within 25 μs.

6. References

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