New Ramp-reset Waveform for Fast Addressing in AC-PDPs

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Abstract

We present new ramp-reset waveforms that realize fast addressing in AC-PDPs. These waveforms distort the distribution of wall charges on the surface of a phosphor layer: hence, the enhanced electric field helps to ignite a cell faster. They also reduce the black luminance: the divide of erasing ramp down discharges into two parts, i.e. a surface discharge and a vertical discharge, makes lower luminance.

1. Introduction

PDPs are most promising for large size displays, but have some problems of cost and performances. One of solutions is a single scan technology already used in VGA scale PDPs. However, it was regarded as unusual in XGA or higher resolution PDPs because of a shortage of addressing time especially in AC-PDPs using the ADS scheme [1] and ramp-reset setups [2][3].

Most of AC-PDPs adopt ramp-reset setups for a reliable driving and a better image quality. The behavior of a ramp-voltage setup has originated from "the dynamic of the ramps" [4][5]: it allows lower address voltage and achieves lower black luminance. In recent years, the hexagonal voltage threshold curve of ramp voltages in three electrodes model was developed [6]~[8]: it helps to understand and design the ramp-reset waveform. It also gives some ideas of reducing the addressing time in the case of the ramp-reset waveforms disclosed in [2][3], which is composed of two periods of writing and erasing ramping voltages.

These waveforms certainly show better addressing characteristics and lower black luminance, but they are not so fast enough to apply a single scan at higher resolution PDPs: because they utilize a relatively uniform distribution of wall charges, the electric field does not much concentrate. Moreover, the voltage levels, act as a limitation, hardly make any further improvement in addressing speed.

In this paper, we suggest new ramp-reset waveforms fast addressable in surface discharge AC-PDPs. Our waveforms are composed of one writing ramp period and two erasing ramp periods. We named them "Dual Discharge mode Ramp-reset" (DDR) waveforms. We tried to overcome the limitation of voltage levels, and noticed that precise control of wall charges could give an opportunity to increase addressing speed: the fact that the non-uniform distribution of wall charges affects firing voltage was predicted in [9],[10]. Thus, we are focusing on finding the way to control wall charges effectively.

We prepared 42" XGA 1024x768 panels to examine the performances of several ramp-reset waveforms. The photo-multiplier-tube was used to detect lights from the panels: a single dot pixel is lit up with no neighboring cells ON to exclude priming effects [11]. Then, the converted light signals were sent to the digital oscilloscope and their histograms were analyzed. We regarded stochastic features of histograms in address discharge time lags as address discharge jitters, i.e. addressability. In section 2.1, we will consider addressability and the limitations of the previous works. In section 2.2, we will present new ramp-reset waveforms. Finally, in section 3, discussions will follow.

2. Experimental results

2.1 Effect of ramp voltages on address jitters

At first, we applied a well-known reset waveform in Figure 1 to examine the relations between address discharge jitters and ramp-reset voltage levels.

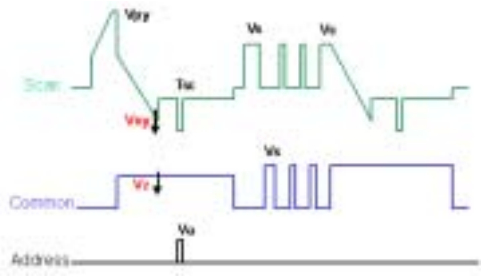


Figure 1 Conventional waveform

We fix the sum of two voltage levels, |Vny| and |Vz|. Equation (1) shows this constriction.

$$|Vny| + |Vz| = fixed. \quad (1)$$

This condition makes the wall voltage across the sustain gap kept almost zero while holding the wall potential of a phosphor layer nearly equals |Vny|. Control of wall voltages with (1) is possible by simultaneous discharges of ramp-reset waveform [6],[8]. Then we measured the address discharge lags five thousand times varying negative going Vny down to -175V and holding the above constriction.

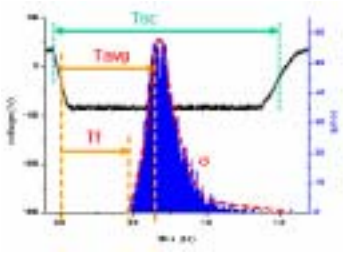


Figure 2 Distribution of address discharge lags

As previously mentioned in the introduction, we adopted statistical procedures to analyze the histograms of address discharge lags. Figure 2 shows a typical histogram of address discharge time lags. We now introduce Z value in order to compare the addressing capability of each histogram. The definition of Z value is

$$Z = \frac{T_{sc} - T_{avg}}{\sigma}. \qquad (2)$$

T_{sc} is the width of a scan pulse, T_{avg} is the average value and σ is the standard deviation of a histogram, respectively. Higher Z value means better address-ability.

Figure 3 shows the result of our first experiment: the dependence of Z value on negative going Vny. It shows that address jitters are getting shorter and saturated as negative going Vny goes more negative. This phenomenon means that positive wall charges on the surface of the phosphor layer gradually diminish as Vny goes more negative. Therefore, the probability of instability due to the loss of wall charges in addressing period decreases.

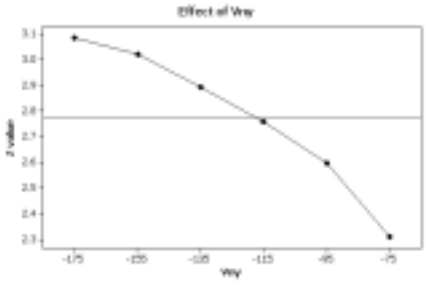


Figure 3 Dependence of Z value on Vny

2.2 Design of new ramp-reset waveforms

We obtained some information from the previous result. It was useful to reduce wall charges on the bottom of a cell for better addressability, but there was a limitation. We thought that control of wall charges on the MgO surface over the scan electrode as well as on the surface of the phosphor layer could improve the performances further more. From the concept of simultaneous control of wall charges, we designed a new ramp-reset waveform: Dividing an erasing ramp discharge into two parts by discharge modes in time order improves addressability and reduces the black luminance.

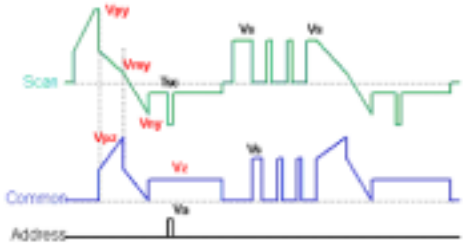
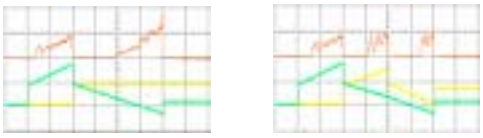


Figure 4 the DDR waveform

Figure 4 represents the DDR (Dual Discharge mode Ramp-reset) waveform. The DDR waveform has an erasing ramp period of successive surface and vertical discharges: the surface discharge between two sustain electrodes and the vertical discharge between a scan electrode and an address electrode. Figure 5 shows IR emissions from each waveform. In Figure 5(b), DDR has divided erasing ramp discharges according to discharge modes contrary to the conventional one. This divide of discharges certainly reduces the black luminance.



(a) Conventional ramp-reset (b) DDR ramp-reset

Figure 5 IR emissions of ramp-reset waveforms

However, we encountered an obstacle applying the above DDR waveform to the large size panels because of large panel capacitance of almost one hundred nano-Farads. Two ramping down phase of scan voltage cannot hold Vmy when abrupt change in common electrode voltage level from Vpz to Vs occurs: capacitance coupling between scan and common electrodes is the reason. Therefore, we have to re-design DDR and Figure 6 shows this modified DDR with Vpz ramping down to zero. Nevertheless, this waveform still has a problem of requiring additional Vpz power supply.

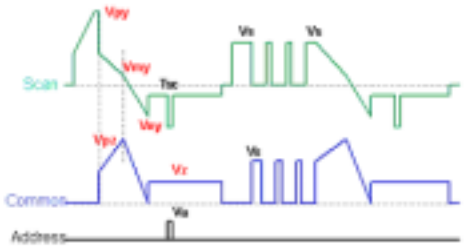


Figure 6 modified DDR

We improved DDR again eliminating the ramp up Vpz of waveform applied in common electrode. Figure 7 represents the simple DDR waveform. We compared the performances of three types of the DDR waveforms. Finally, we concluded that their performances have no difference in addressability and the black luminance because ramp down phase has the same effect on the panels.

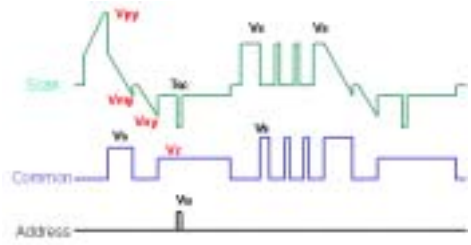


Figure 7 simple DDR

2.3 Result of the new ramp-reset waveform

We are now focusing on an operation of simple DDR in Figure 7. The surface discharge in the first step of erasing ramp has the similar effect with the result of Figure 3 in section 2.1. Meanwhile, the next consecutive vertical discharge could control wall charges on both sides of scan and address electrodes simultaneously.

Table I shows the result of the comparison between the conventional and DDR. We used 1.3us of a scan pulse and the delay-time of 1ms prior to applying the scan pulse. The voltage level Vmy in simple DDR is set to be -50V. In Table I, DDR shows better performances: lower black luminance of 10% as well as higher addressability of 45%.

Table I Comparison between ramp waveforms

Waveform	Vmy (V)	Vz (V)	Black luminance (cd/m2)	Tavg (us)	T1 (us)	t (us)	Z	%
Reference	-95	190	0.18	0.816	0.480	0.186	2.62	100%
	-175	90	0.18	0.772	0.470	0.169	3.12	119%
DDR	-155	110	0.16	0.741	0.450	0.148	3.78	144%

3. Discussions

3.1 Black luminance

We have already shown IR emissions from DDR in Figure 5(b). In the conventional waveform, IR emissions from the erasing ramp period in Figure 5(a) gradually increase with time. DDR is likely to cut-off strong emissions from erasing ramp edge: the sum of IR emissions from surface and vertical discharges in DDR is weaker than that of the erasing ramp phase in the conventional waveform.

3.2 Fast addressing

We calculated wall charges and electric fields using the two-dimensional simulator SIPDP-AC™ [12] to support our experimental results.

Figure 8 shows distributions of charge densities after each ramp-reset waveform. DDR distributes positive wall charges more non-uniformly over the phosphor layer: wall charges on the phosphor layer below the scan electrode were erased more than those of the conventional waveform.

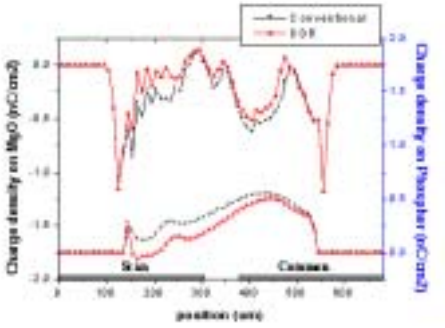


Figure 8 Charge density after ramp-reset

Figure 9 represents the electric field intensity of each waveform perpendicular to the MgO surface at an addressing moment. In DDR, the electric field intensity is greater than that of the conventional. It means that the DDR waveform has a chance to trigger a faster discharge than the conventional one.

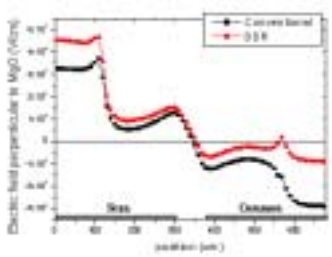


Figure 9 Electric fields at addressing period

Figure 10 shows address discharge currents at address periods. DDR shows faster addressing than the conventional expected in Figure 9.

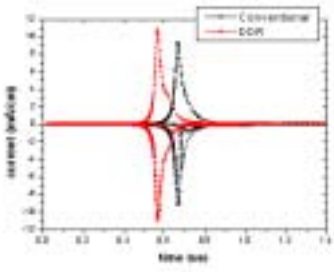


Figure 10 addressing discharge at addressing period

In the real world, address jitters do not follow exactly the simulation results because of statistical uncertainty. In general, discharge time lags have a stochastic feature and follow Laue's expression [13].

$$N / N_0 = 1 - \exp\left\{-(t - t_f)/\tau_s\right\} \qquad (3)$$

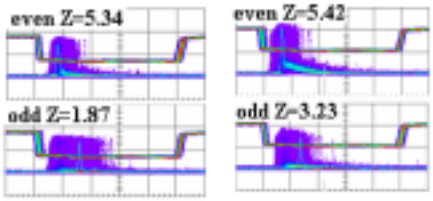
N is the number of discharges after time t in N_0 trials and t_f is the formative time lag. The statistical time constant, τ_s is inversely proportional to the discharge probability, P_0 and seed particle density, n_0.

$$\tau_s \propto 1/P_0 n_0 \qquad (4)$$

The discharge probability P_0 is dependent on the potential distribution as well as materials and gas properties. The formative time is also dependent on potential distribution. In Table I in section 2.3, DDR affects both the formative time lag and the standard deviation. Therefore, we concluded that DDR is likely to generate more seed particles as well as to control the potential distribution on the phosphor layer. More priming particles seem to affect align-robust addressing of DDR in following section.

3.3 Align-robust addressing

As mentioned in pervious section, DDR can reduce misalign effects of bad manufacturing better than the conventional waveform. Figure 11 shows that DDR compensate misalign effects greatly. In this case, the panel has been misaligned several tens of microns.



(a) Conventional **(b) DDR**

Figure 11 misalign effects of a cell; DDR reduces misalign effect greatly.

4. Conclusions

We investigated the relations between address discharge jitters and the ramp-reset conditions. We found wall charges on the surface of a phosphor layer dominate addressability and saturation of jitters is the limitation in the conventional waveform. We proposed new ramp-reset waveforms as well as a statistical method to analyze performances of them. New ramp-reset waveforms are fast addressable and align-robust so that they realize a single scan driving at higher resolution PDPs.

5. References

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