Dual-Slope Ramp Reset Waveform to Improve Dark Room Contrast Ratio in AC PDPs

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Abstract

A new dual-slope ramp (DSR) reset waveform is proposed to improve the dark room contrast ratio in AC-PDPs. The proposed reset waveform has two different voltage slopes during a ramp-up period. The first voltage slope is lower than the conventional ramp voltage slope, causing a reduction in the background luminance, whereas the second voltage slope is higher than the conventional ramp voltage slope, causing an increase in the background luminance. Thus, a bias voltage is also applied during the second voltage-slope period to adjust the background luminance and address discharge characteristics. As a result, the proposed dual-slope reset waveform can lower the background luminance, thereby improving the high dark room contrast ratio of an AC-PDP without reducing the address voltage margin

1. Introduction

Plasma television is believed to be a promising candidate for large area (> 40 inch), self-emitting, digital high definition home theater TVs. Therefore, improving the image quality generated by a plasma TV is a critical issue for current PDP technology. In particular, improving the dark room contrast ratio is a very important factor contributing to the high image quality required for a plasma home theater TV. As a result, a lot of research has focused on reducing the background luminance during a reset period [1, 2, 3]. The voltage slope during a ramp-up period also has a considerable affect on the background luminance as well as the address discharge characteristics. However, improving the dark room contrast ratio by controlling the voltage slope during a ramp-up period is difficult, since the conventional ramp reset waveform only has one voltage slope during a ramp-up period.

Accordingly, this letter proposes a new dual-slope ramp (DSR) reset waveform to improve the dark room contrast ratio in AC-PDPs, where the proposed reset waveform has two different voltage slopes during a ramp-up period. In addition, a bias voltage is also applied during the second voltage-slope period to adjust the background luminance and address discharge characteristics.

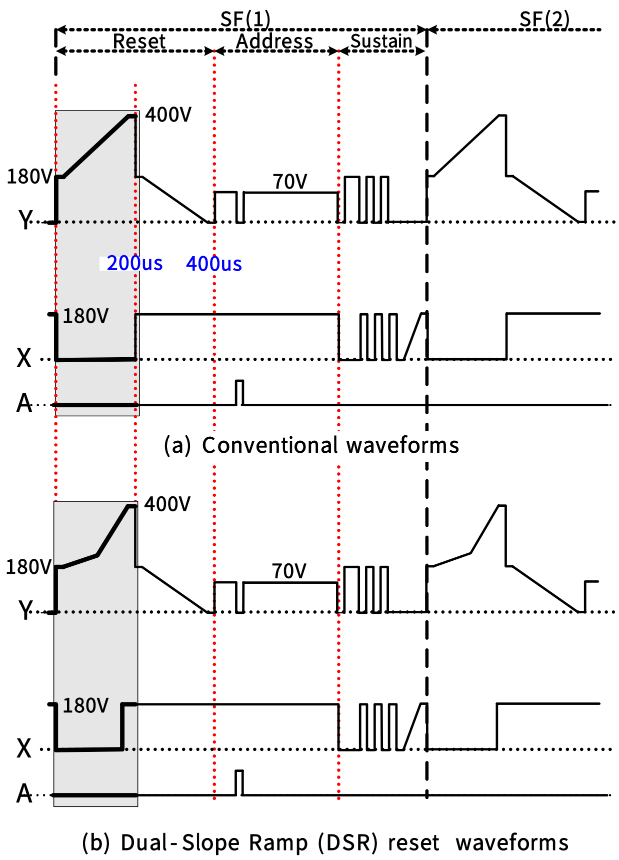


Fig. 1. Driving waveforms employed in current study, including (a) conventional ramp reset and (b) proposed dual-slope ramp (DSR) reset waveforms.

2. Experimental setup

A typical 7-in. AC-PDP was used as the test panel with a conventional three-electrode coplanar structure. Figs. 1 (a) and (b) show the driving waveforms employed in the current study, including (a) the conventional ramp reset and (b) proposed DSR reset waveforms. As shown in Fig. 1, the proposed reset waveforms has a dual voltage slope instead of one voltage slope during a ramp-up period. The first voltage slope of the DSR waveform is lower than that of the conventional ramp reset waveforms, whereas the second voltage slope of the DSR waveform is higher. Furthermore, a bias voltage is applied to the sustain (X) during a ramp-up period, especially during the second voltage-slope period, whereas the address (A) electrode remains grounded during a reset-period. To compare the reset discharge characteristics of both the conventional and proposed reset waveform, the IR emissions were observed using a highly sensitive light detector (Hamamatsu, C6386).

3. Results and Discussion

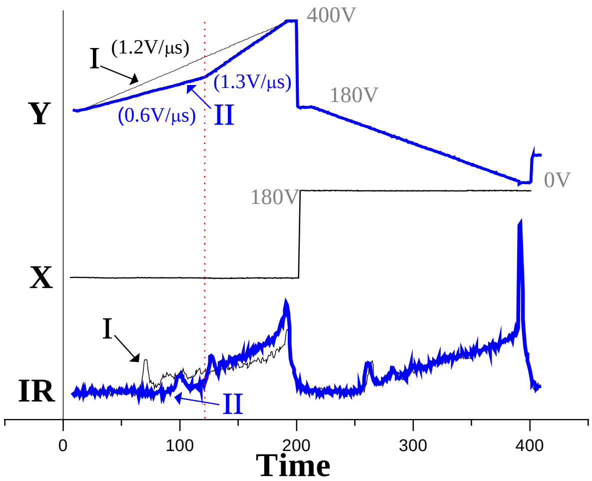
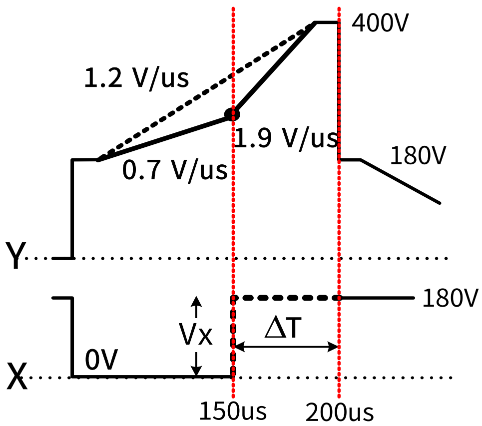
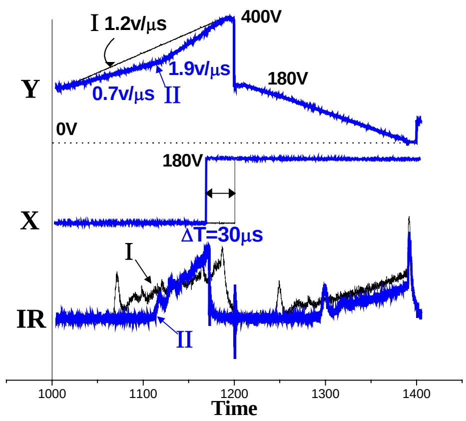


Fig. 2. Changes in IR emission waveforms when applying conventional (Ⅰ) and proposed DSR (Ⅱ) reset waveforms.

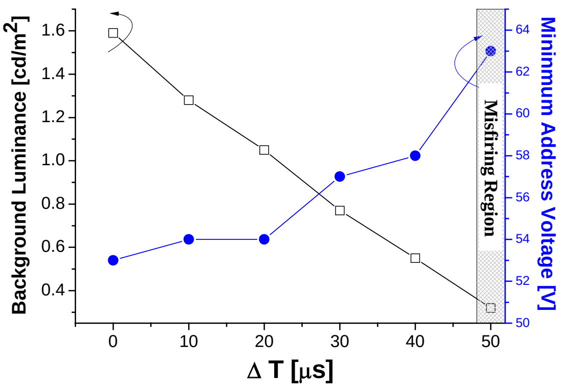
Fig. 2 shows the changes in the IR (828 nm) emission waveforms in the case of applying the conventional (Ⅰ) and proposed DSR (Ⅱ) reset waveforms at a zero X-bias voltage during a ramp-up period. As shown in Fig. 2, with a zero bias voltage at the X electrode, the first voltage slope (=0.6 V/μs) was lower than the conventional ramp voltage slope (=1.2 V/μs), thereby reducing the background luminance, whereas the second voltage slope (=1.3 V/μs) was higher than the conventional ramp voltage slope, thereby increasing the background luminance. Thus, to reduce the background luminance during the second voltage slope-period, the increase in the voltage rate between the X and Y electrodes needs to be minimized by applying an X-bias voltage. Since the application time and amplitude of the X-bias voltage can affect both the background luminance and the address discharge characteristics, the biasing condition of the X-bias voltage must be determined very carefully. Fig. 3 (a) shows the X-bias voltage applied during the second voltage slope-period, where ΔT represents the application time of the X-bias voltage, which is a very important parameter for both the background luminance and the address discharge characteristics. Fig. 3 (b) shows the changes in the IR (828 nm) waveforms in the case of applying the conventional reset and proposed DSR reset waveform with an X-bias voltage of ΔT=30 μs, respectively. The voltage slope for the conventional reset waveform was 1.2 V/μs, whereas for the DSR reset waveform, the first voltage slope was 0.7 V/μs and the second voltage slope was 1.9 V/μs. Unlike the results in Fig. 2, with an X-bias condition of ΔT=30 μs, the background luminance was reduced during the second voltage slope-period, as shown in Fig. 3 (b). However, under these conditions, the minimum address voltage also increased, as seen in Fig. 3 (c), which shows the relation between the background luminance and the minimum address voltage with respect to ΔT [3]. As shown in Fig. 3 (c), when increasing ΔT, the background luminance was decreased, yet the minimum address voltage was increased. Accordingly, the optimal condition between the two voltage slopes and the X-bias condition needs to be determined. Figs. 4 (a), (b), (c), and (d) show the changes in the background and minimum address voltage [(c) and (d)] for case 1 (a), where the first voltage-slope period is fixed at T_1= 130 μs, and case 2 (b), where the amplitude of the first voltage slope-period is fixed at V_2 = 85 V under constant X-bias conditions (*i.e.*, Δ T = 28 μs, V_x = 180 V). In case 1, the amplitude during the first voltage-slope period, *i.e.* ΔV_1, varied from 60 to 140 V at intervals of 20 V, whereas in case 2, the time interval during the first voltage-slope period, *i.e.* ΔT_2, varied from 75 to 110 μs.



(a)

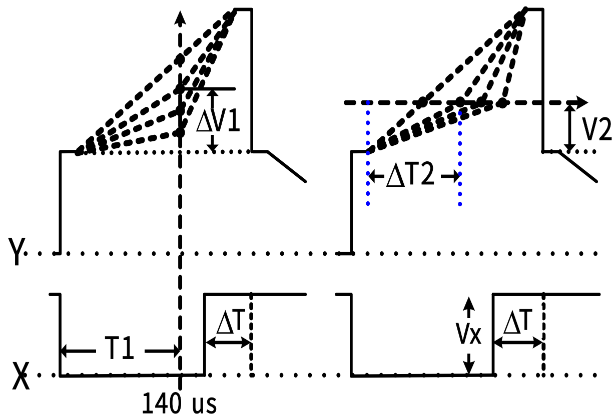


(b) Δ T = 30 µs

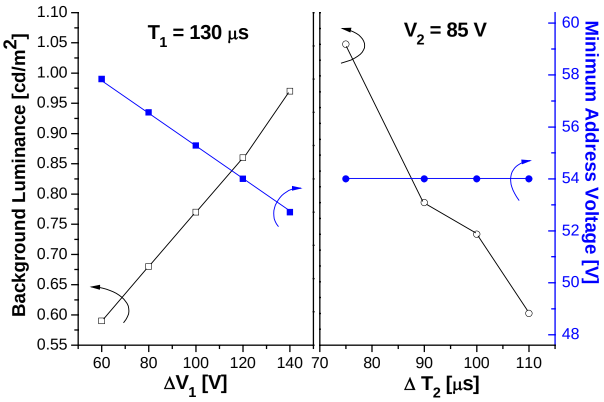


(c)

Fig. 3. (a) X-bias voltage applied during second voltage-slope period, where ΔT means application time of X-bias voltage, (b) changes in IR emission waveforms when applying conventional and DSR reset waveform with X-bias of ΔT=30 µs, and (c) changes in background luminance and minimum address voltage with respect to ΔT.



(a) T_1= 130 µs (b) V_2 = 85 V



(c) T_1= 130 µs (d) V_2 = 85V

Fig. 4. Changes in background and minimum address voltage [(c) and (d)] for case 1 (a), where first voltage-slope period is fixed at T_1= 130 µs, and case 2 (b), where amplitude of first voltage-slope-period is fixed at V_2 = 85 V.

As shown in Fig. 4 (c), when Δ V_1 was increased, the background luminance was also increased, yet the minimum address voltage was decreased. However, as shown in Fig. 4 (d), when the Δ T_2 was increased, the background luminance was decreased, but the minimum address voltage remained almost constant, where the background luminance with the proposed DSR reset waveform was reduced to 43 % of the background luminance generated by the conventional ramp reset waveform without reducing the minimum address voltage. Consequently, when adopting the DSR reset waveform, the dark room contrast ratio was improved by about 77 %.

Table. 1. Performance comparison between conventional and proposed DSR reset waveforms.

	Conventional Reset Waveform	Proposed DSR Reset Waveform	
Ramp voltage slope	Single slope	Dual slope	
Voltage slope during ramp-up period	1.2 V / µs	First slope	Second slope
		0.7 V / µs	1.9 V / µs
Vbias during ramp-up period	0 V	0 V	180 V
Voltage slope during ramp-down period	1.2 V / µs	1.2 V / µs	
Background luminance	1.58 cd/m^2	0.89 cd/m^2 (43%)	
Display luminance	278 cd/m^2	278 cd/m^2	
Dark room contrast ratio	175.94	312.35 (77%)	
Address minimum voltage	54 V	54V	
Common conditions	10 reset periods (=10 sub field)/frame 7 inch test panel (42Bus) Vreset : 400V Vscan : 70V Vsustain : 180V No selective reset		

4. Conclusion

A new dual-slope ramp (DSR) reset waveform was proposed to improve the dark room contrast ratio in AC-PDPs. The proposed reset waveform has two different voltage slopes during a ramp-up period. The first voltage slope is lower than the conventional ramp voltage slope, thereby reducing the background luminance, whereas the second voltage slope is higher than the conventional ramp voltage slope, thereby increasing the background luminance. Thus, a bias voltage is also applied during the second voltage slope period to adjust the background luminance and address discharge characteristics. When adopting the optimized DSR reset waveform, the dark room contrast ratio was improved by about 77 %. Consequently, the proposed DSR reset waveform can improve the dark room contrast and support a higher image quality for AC-PDPs.

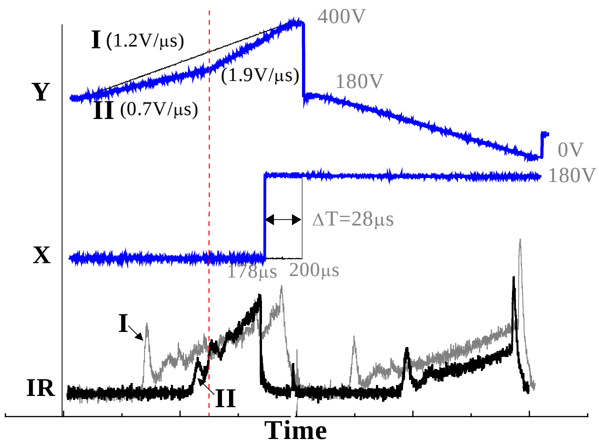


Fig. 5. Changes in IR emission waveforms when applying conventional and optimized DSR reset waveforms.

5. References

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