A New Address-While-Display Driving Method using the Short Ramp Reset Pulse (SRR) for High Contrast ratio and Wide Address Margin

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Abstract

We propose a new address-while-display (AWD) driving method to obtain a high contrast ratio and a wide driving margin which is composed of a short ramp reset period, a sustain period and an address period as the basic unit. The short ramp reset (SRR) pulse made it possible to assure the wide operating voltage margin and minimize the background luminance by redistributing the wall charges between address and scan electrode. As a result, a high dark room contrast ratio of 10000 to 1 could be obtained with a wide operating voltage margin of 40V for stable address.

1. Introduction

The alternating current plasma display panel (AC PDP) is one of the promising flat panel display devices with the sizes larger than 40-in diagonal and is under active development for its application to high definition television (HDTV) in which the address and display separation (ADS) method has been widely used as one of the major driving schemes [1]-[2]. However, as the display size becomes larger and its resolution increase, the ADS driving method using a long time of ramp reset waveform becomes inappropriate, since it will be difficult to provide a sufficient time to display images when the number of scan lines increases.

In the case of address-while-display (AWD) method, strong pulse reset schemes had been mainly used, which involves self-erasing discharges and unwanted strong background light emission during the reset period, so that the operating voltage margin was narrow and the contrast ratio was lower than those of ADS method[3]-[5]. There have been many researches to find appropriate AWD driving techniques to secure a high luminance, high contrast ratio and wide operating voltage margin for high picture quality AC PDP [6]-[7].

In this paper, we propose a new AWD driving method using a short ramp reset (SRR) pulse with a short pulse erase (SPE) at the end of sustain period which resulted in a high contrast ratio with a wide operation voltage margin.

2. New Waveform Design

The driving waveform of an AC PDP is usually composed of the reset, addressing and sustain period. In general, the basic unit named 1T, 1H or 1subfield has the above three periods sequentially. In this work, we divided the conventional unit into each functionalized blocks and then took them as basic units. These combinations of the functionalized blocks make the reset, addressing and sustain period.

As shown in Fig. 1, the voltage waveform being applied into the common electrode is composed of the basic two driving units *B* with biased voltage and D_x period with display pulses, and that of scan electrode have *R* with ramp biased pulse, *T* with ground voltage level, *S* with scan pulses and D_y period with display pulses. All have the same 30us period. Scan lines are divided into two blocks according to the 180 degree phase shift of voltage waveform applied to X electrode. One scan block of the *S* and *B* period have 24 scan lines with each scan pulse width of 1.25us. First 12 scan pulses are applied in the $(4n+1)_{th}$ line and next 12 scan pulses are applied in the $(4n+3)_{th}$ line. The other scan block is positioned to the $(4n+2)_{th}$ and $(4n+4)_{th}$ line like the preceding.

12 sub-fields constituted 1 TV frame and every sub-field has its own reset period. The numbers of sustain blocks were set as 1*, 1, 1, 3, 5, 9, 17, 31, 47, 47, 47, and 47 in sequence. This arrangement is a modified one from the conventional binary-bit-number com-position with eight subfields for the newly suggested waveform. Subfield 1* has a short pulse erase scheme at the first of sustain period to express the low luminance level. The sustain pulse width were set to be 5μs each. The experiment has been performed only when the stability of the reset period is satisfied.

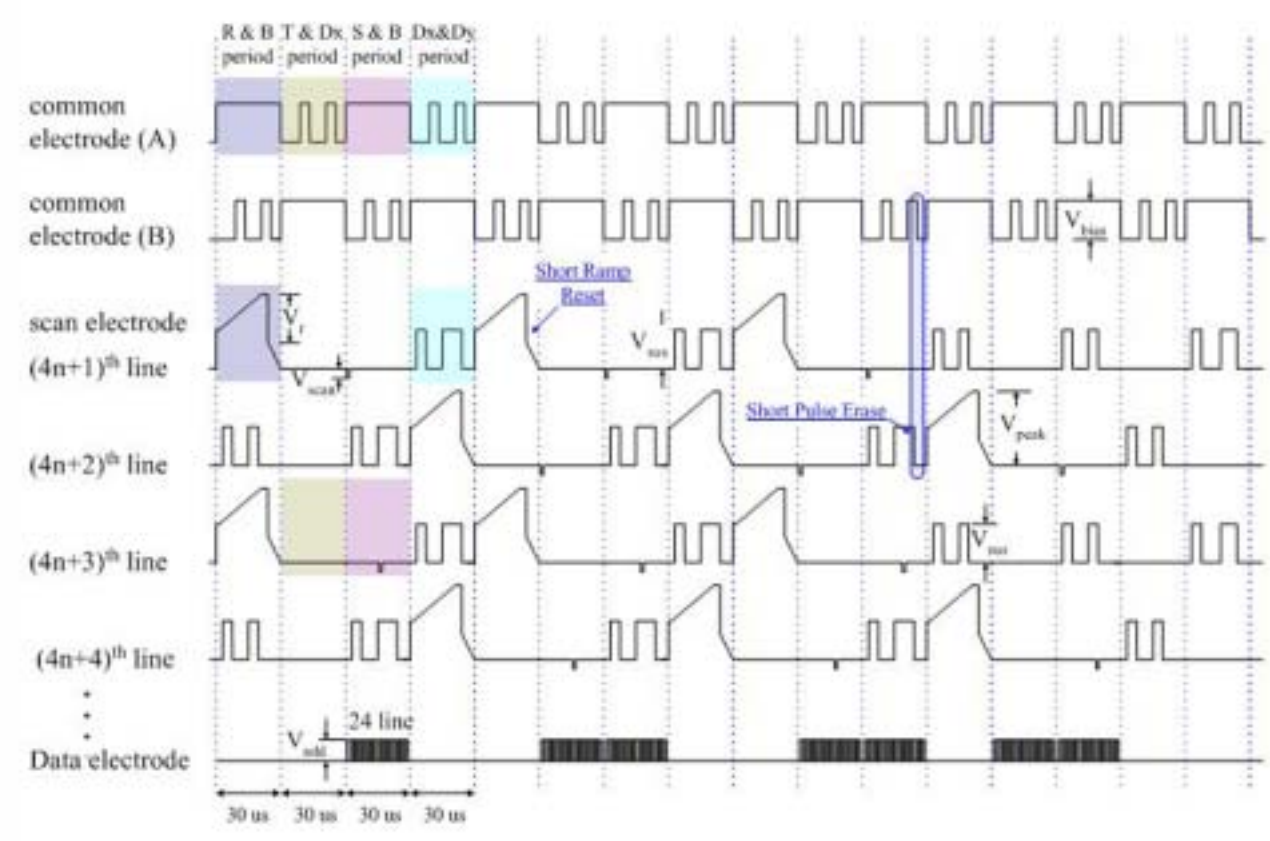

Fig. 1 Drive voltage waveform of the newly proposed method

Fig. 2 shows electrode connections of the panel. The 540 common and scan electrodes in the upper half of the panel are grouped into 2. That is also connected with another address driver block in the lower half for a 1920 x 1080 Full-HD dual scan panel.

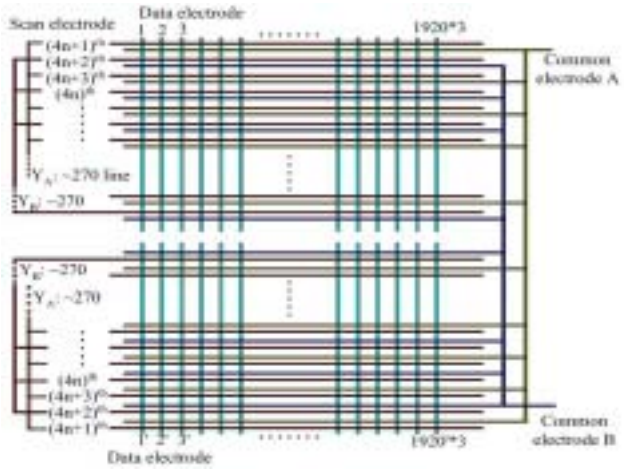

Fig. 2 Electrode connections for a 1920 X 1080 pixel panel

In our experiment, 7.5inch test panel was used with 42inch XGA format having 1024 x 768 pixels. Gas mixture of Ne-Xe(4%) to Ne-Xe(14%) 400-torr were employed.

3. The Experimental and Result

The operating margin of a new AWD method was compared with that of the conventional ADS method using ramp reset and the peak luminance and the dark room contrast ratio was obtained in the optimized voltage condition.

3. A Background luminance

As shown in the Fig. 1, the short ramp reset (SRR) is applied at the beginning of each subfield. This SRR pulse makes the wall charges redistributed between scan (Y) and address (A) electrode. It was reported that background luminance by the ramp reset between Y and A electrode is lower than that between Y and X electrode [8]. In our scheme, there are two sustain pulses overlapping with same voltage at the end of sustain period as shown in Fig. 3. But the voltage applied to the Y electrode goes down to zero just

before the X electrode does at t3, so that the wall charges near the gap between surface two electrodes are erased and then the negative wall charges on the Y and X electrode and the positive wall charges on the A electrode are accumulated during the SRR period.

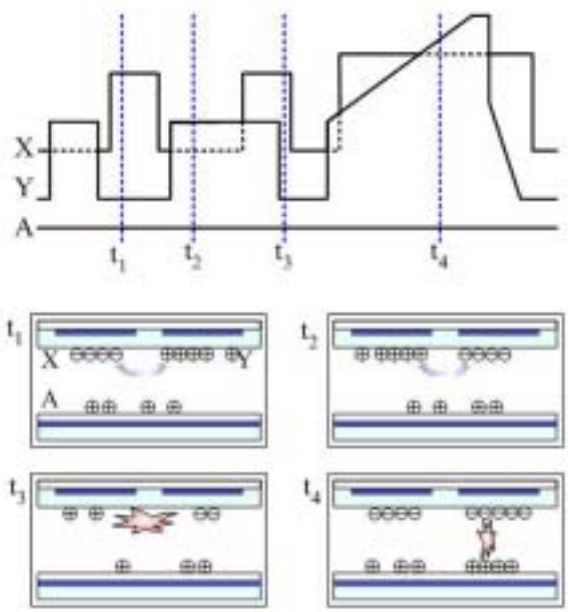

Figure 3. Wall charge diagram in SRR and SPE period

This short pulse erase and SRR could reduce the unwanted background light due to the excessive change of wall charge and set up the wall charges in each pixel to the appropriate states and we were able to obtain a low level of 0.065cd/m^2 of background luminance.

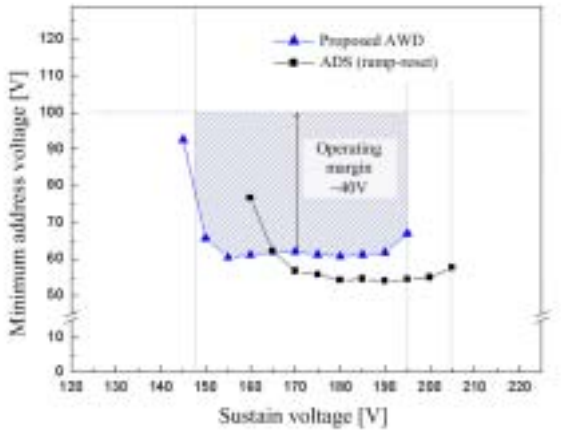

Figure 4. Operating voltage margin for sustain and address pulse voltages

3. B Driving Voltage Characteristics

We could obtain a wide operating voltage margin with the use of the SRR and SPE pulse scheme. Fig. 4 shows the minimum address voltage according to the proposed new AWD scheme compared with the normal ramp reset ADS scheme. In case of the proposed AWD method, the minimum address voltages according to the increase of sustain voltage are uniformly around 61V and similar to that of the ADS scheme. Moreover, the sustain voltage range of the proposed AWD method is lower by about 10V.

In the general AWD driving scheme, |Vscan|+Vadd-min. corresponded to the firing voltage between Y and A electrode because of no use of wall charges. Fig. 5 shows the operating voltage margin for scan and address pulse voltage. As the absolute value of scan pulse voltage increases, minimum address pulse voltage decreases together with maximum address pulse voltage. Display discharge always took place at 64V and more. The 40V of operating margin could be obtained. Table 1 shows the driving conditions and background luminance of the two methods.

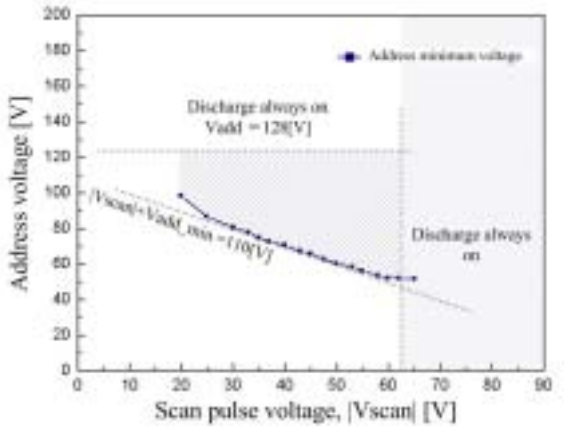

Figure 5. Operating margin for scan and address pulse voltages

3. C Dependency on various Xe contents

Fig. 6 shows the address minimum voltage according to the variation of Xe contents. As the Xe contents increase, the address minimum voltage is increase slightly and the sustain voltage range also shifts to higher voltage level by about 5 ~ 10V respectively. But the rate of increase in newly proposed AWD driving scheme compared is smaller than those of the ramp reset ADS driving scheme in the address minimum voltage as shown in Fig. 7.

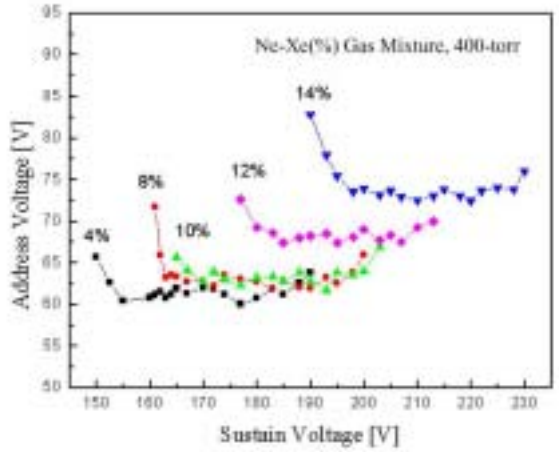

Figure 6. address minimum voltage to variation of Xe contents

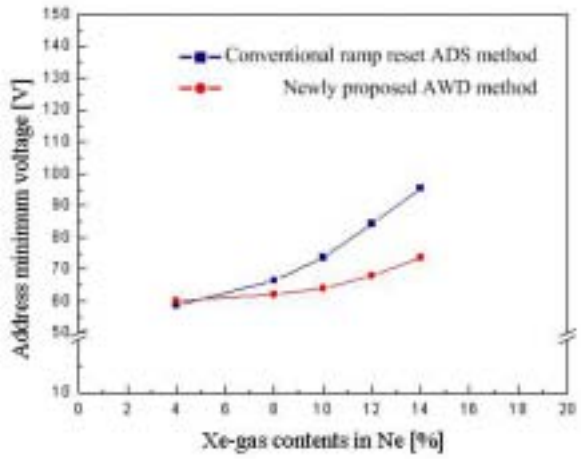

Figure 7. Comparison of address minimum voltage

We could obtain a wide operating margin of 40V for 4, 8 and 10% Xe contents and for 30V for 12 and 14% Xe contents.

4. Conclusion

In this work, we proposed a new Address-While-Display using the short ramp reset (SRR) pulse to obtain a high contrast ratio and wide operating margin. Newly proposed AWD driving method also shows possibility to use for the PDP with high Xe contents. We could achieve the darkroom contrast ratio of 10000: 1, and 40V of the address voltage margin. The detailed optimized operating voltage conditions are illustrated in TABLE I.

TABLE 1

Optimized driving conditions and characteristics

	Conventional ADS method using Ramp reset	Proposed New AWD method using Short ramp reset
Peak reset voltage	390V	340V
Rise/Fall ramp slope	1.5V/μs ‖ 1.2V/μs	8V/μs ‖ 40V/μs
Peak L.(1000pulses)	720 cd/m^2	694 cd/m^2
Background luminance	1.446 cd/m^2	0.065cd/m^2
Contrast ratio	468 : 1	10600 : 1
Reset Time	360 μs	30 μs
Voltage condition :	$V_{SUSTAIN}$ = 200,$V_{SCAN(Y)}$ = 70, $V_{ERASE(Y)}$ = 200$V_{ERASE(X)}$ = 180,	$V_{SUSTAIN}$ = 180,/-$V_{SCAN(Y)}$ = 50 $V_{ERASE(X)}$ = 180,
60 frame / second, 8 subfield / frame , 7.5inch test panel., XGA resolution		
Ne-Xe(8%), 400-torr, Address margin : tested with full white pattern		

5. Acknowledgements

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6. References

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