Analysis and Remedy of TFT Based Current Mode Logic Circuit Performance Degradation due to Device Parameter Fluctuation

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Abstract
We report the influence of the threshold voltage and mobility fluctuation in TFT on current mode digital circuit performance. We found that the threshold voltage showed more serious circuit malfunction. We studied new circuit configuration for improvement.

1. Introduction

It is widely accepted that the flat panel displays soon integrate most of the driving electronics on glass substrate by using low temperature polysilicon (LTPS) thin film transistors (TFTs). Already, flat panel displays for mobile applications commonly contain TFT based scan driver as well as data drivers.

Even though the properties of LTPS TFTs have been improved drastically, compared to the bulk MOSFET, the TFT circuit performance is generally low and less reliable. To enhance the speed of circuit operation we have introduced simplified current mode inverter as shown in Fig. 1. It is made only of pTFTs for higher hot carrier immunity and simpler process. It does not have current mirror since TFTs can not be used to make accurate current source because of threshold voltage fluctuation. Thanks to this approach, the logic gate design is as simple as CMOS design and we achieved more than 50% performance improvement with compatible power consumption. Furthermore, we were able to reduce the chip size by more than 20% since CML gates used lower logic swing and required less current driving capabilities.

We designed a current mode shift register based on the current mode inverter and its schematic is shown in Fig. 2. Our simulation results of the shift register had shown 72% increase in speed, 45% decrease in chip area at the cost of 40% higher power consumption.

It is the purpose of this paper to analyze the effect of device parameter fluctuation such as threshold voltage and carrier mobility. After the analysis, we will propose a improved circuits which are less sensitive to the parameter variation.

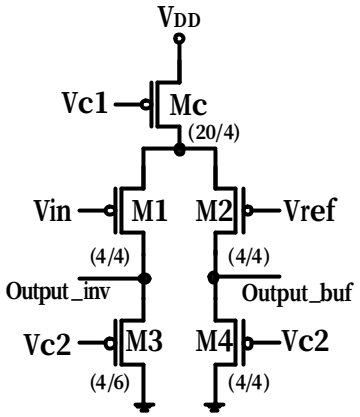

Fig. 1 All pTFT current mode inverter

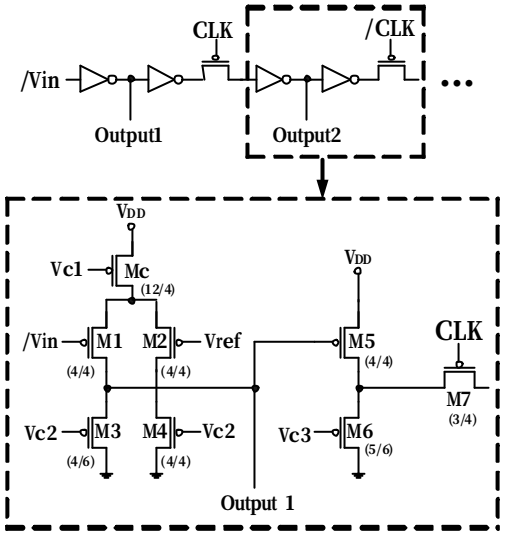

Fig. 2 Current Mode Shift Register

2. Effects of Device Parameter Variation

Even though the threshold voltage fluctuation affects less in digital circuit performance, we found it had caused circuit malfunction due to imbalance of propagation delay. This situation

was most noticeable in multistage shift registers where signal stopped to propagate.

To analyze the effect of the threshold voltage fluctuation, we simulated CML inverter/buffer gate with threshold voltage variations. The results are summarized in Fig. 3.

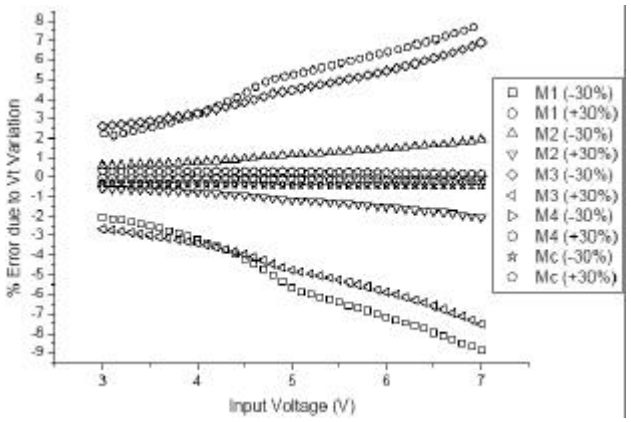

Fig. 3 Transfer characteristic error due to threshold voltage change of -30 or +30% for TFT's in the current mode inverter in Fig. 1

For Mc transistor which acts as a current source, the transfer characteristic of the inverter is independent of the threshold voltage variations. For M2 and M4 which are in the reference side of the inverter affected the transfer characteristics little. On the other hand, Vt fluctuation in the transistors M1 and M3 results serious transfer characteristics change.

From Fig. 4(a) which shows the degree of regenerative property, one can see that the CML inverter has very small margin in the operation range between 4.1 and 6.2 volts. The areas enclosed by the two transfer characteristics are regeneration margin of inverters. When Vt of M1 transistor changed -30%, the operation range is between 4.4 V and 6.1V. On the other hand +30% change results the range from 3.8V and 6.2V. Outside of these operation ranges, the circuit does not regenerate and operation failure may occur.

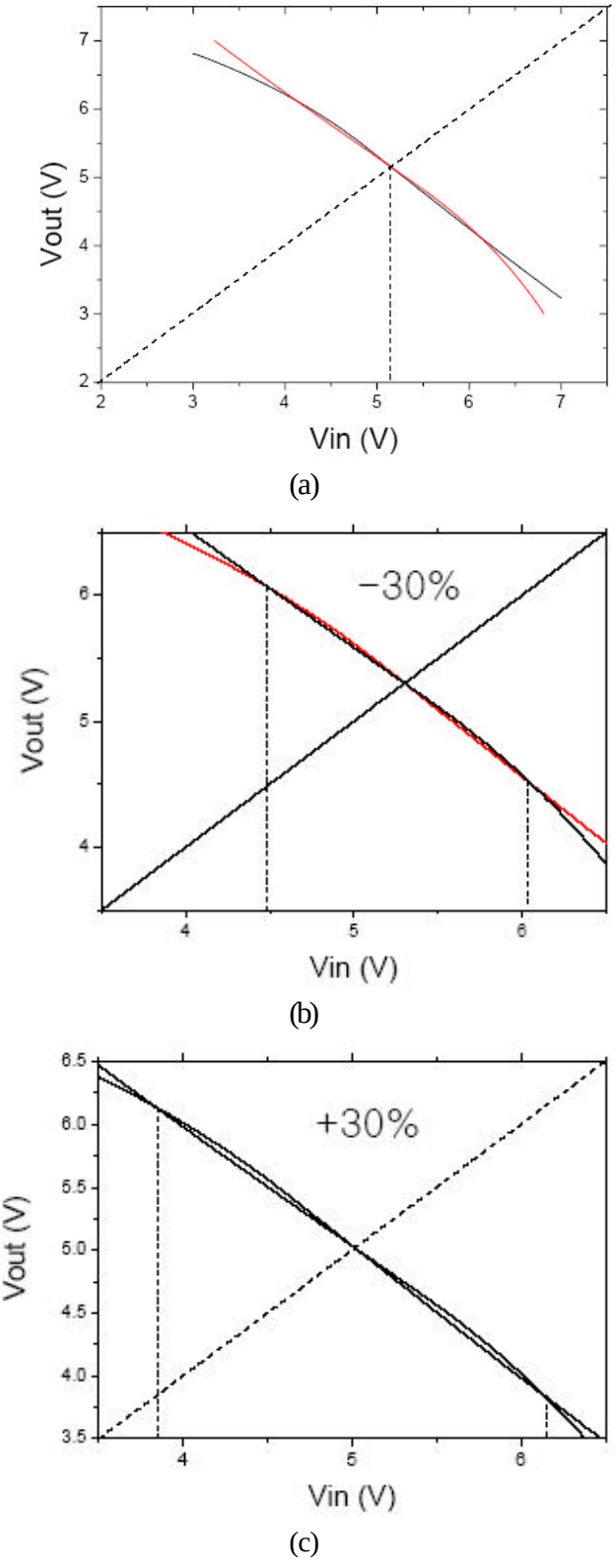

Fig. 4 Regeneration margin of CML inverter with M1 Vt change (a) no change, (b) -30%, (c) +30%

Effectively, mobility variation is similar to Vt fluctuation and one may relate higher mobility to lower threshold voltage in terms of driving current. As expected lower mobility results similar results as higher threshold voltage and vice versa. Also, we found M1 and M3 are more sensitive while M2 and M4 does not affect the characteristics.

3. Improved CML Inverter

It is shown that the CML inverter shows weak nonlinearity and small regeneration margin. Furthermore, when threshold voltage changes the margin and operation voltage range shrink. To obtain enhanced stability against the device parameter variation, we changed to differential input CML inverter as shown in Fig. 5 and its regeneration margin is shown in Fig. 6 (a). One can notice that the regeneration margin is larger than that of Fig. 1.

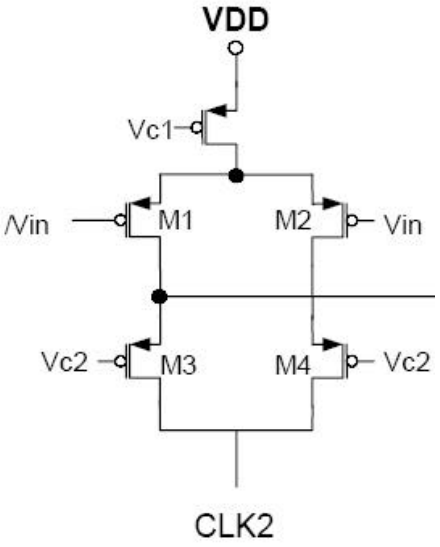

Fig. 5 Improved CML inverter with differential input.

We conducted threshold voltage variation analysis and found that M1, M3 are crucial component while M2, M4 are insensitive to the fluctuation as in the inverters in Fig. 1. The transfer characteristics and/or regeneration margin of the new CML inverter with threshold voltage variation is shown in Fig. 6 (b). There are two unique features. First, regeneration margin remains almost constant even when Vt is changed by ±30%. Second, operation voltage ranges cover all the voltages we used for CML inverters and independent of the device parameter fluctuation.. These facts we observed indicates that the new CML inverter is more robust than the one in Fig. 1.

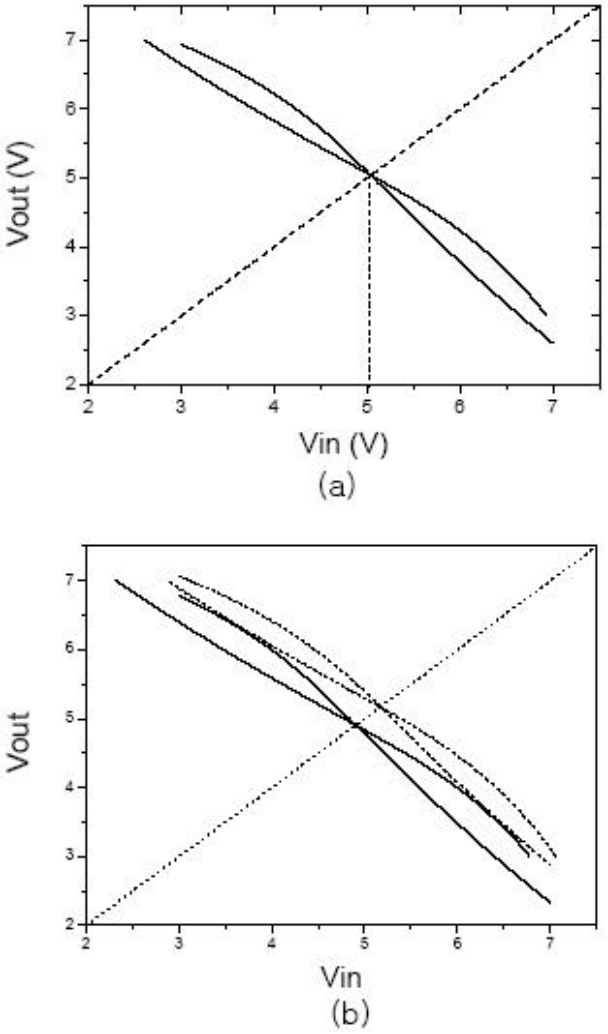

Fig. 6 Regeneration margins of new CML inverter with differential input pair. (a) without Vt variation, (b) ±30% Vt variation (dashed line:-30%, solid line:+30%).

Furthermore, overall performance also improves. First, power consumption of the new inverter becomes lower. This is due to the reduction of static current in M2, M4 current path. Previous CML inverter structure has 15 uA while the improved CML inverter has only 4 uA static current. Second, switching speed is increased. Before, only left current path consists of M1 and M3 turns on and off while right side remains 'ON'. On the other hand, both current paths are

switching in opposite direction and current redistributes more effectively.

4. Performance test

To test the rebustness we have designed two shift registers of Fig. 2 with both reference voltage CML inverters of Fig. 1 and differential input CML inverters of Fig. 5. The simulation results of Vt fluctuation is shown in Fig. 7 which show shift register outputs after each stage.

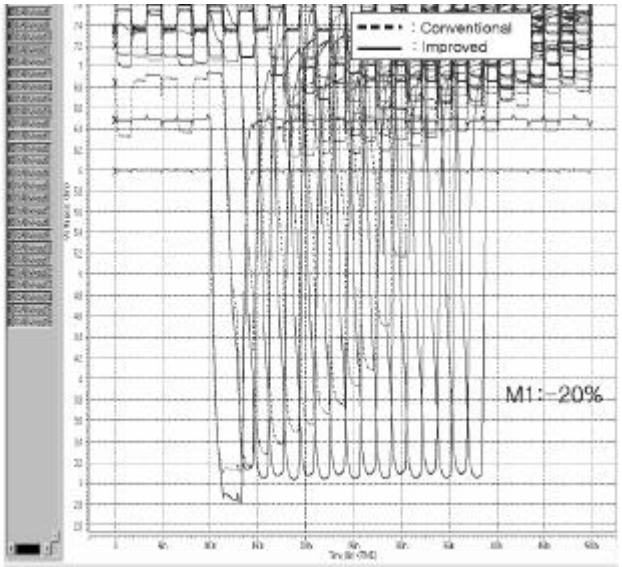

Fig. 7 Output waveform of shift registers (solid line: differential input CML inverter based, dashed line : reference voltage CML inverter based).

The reference voltage CML inverter based shift register works well when Vt is increased by more than 20%. However, when Vt is decreased, its performance deteriorates and signal can't propagate at 20% Vt reduction. One can notice that the output voltage does not drop to the bottom and after each stage, the lowest voltage gets higher. This is closely related to the shrinkage of regeneration margin and operation voltage range discussed in Fig. 4 (b). However, on the other hand, the differential input CML inverter based shift register works well even in this condition and proved to be more robust.

5. Conclusion

We have studied Vt fluctuation effects on our current mode logic gates. And found a modified way of designing CML inverter for better performance and robustness. The new circuit takes advantage of smaller layout, higher speed,and smaller chip size over static CMOS counterpart.

6. Acknowledgements

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