A Data-line Sharing Method for Lower Cost and Lower Power in TFT-LCDs

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Abstract
This paper presents a new data line sharing technique for TFT-LCD panels. This technique reduces the number of data driver IC's to half by having two adjacent pixels share the same data line. This in turn doubles the number of gate lines, which are integrated directly on the glass substrate of amorphous silicon for further cost reduction and more compactness. The proposed technique with new pixel array structure was applied to 15.4 inch WXGA TFT-LCD panels and has proven that the number of driver IC's were halved with nearly 41% circuit cost reduction and 5.3% reduction in power consumption without degrading the image quality.

1. Introduction

Today, TFT-LCD technology has a wide range of application from consumer products such as note PC and TV's to office products such as desktop computer monitors and PDA's. The most critical features of those products are power consumption and cost. Half Column Line Driving (HCLD) method was proposed before to fulfill those requirements [1]. As illustrated in Figure 1, both right and left pixels share the data lines in HCLD method, reducing the number of driver IC's to half. It, however, increases the the number of gate lines twice and therefore increases the number gate driver IC's twice [2],[3]. To overcome these problems, this paper proposes a new method to reduce the driver IC's by half and at the same time eliminating the gate driver IC's by integrating them on the amorphous silicon glass substrate. It also adopts the column inversion for the reduction in power consumption and new TFT array to prevent vertical crosstalk.

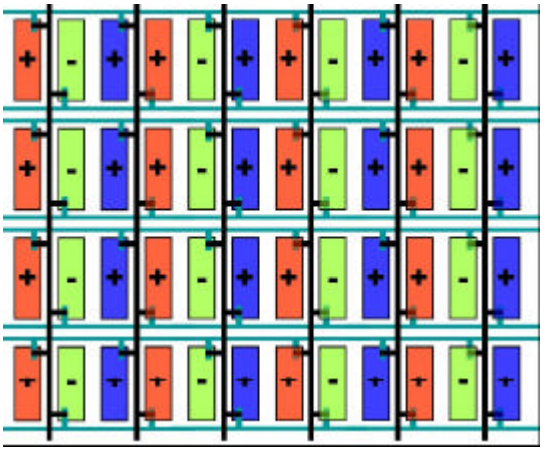

Figure 1. The TFT Array for Conventional HCLD

2. Results

2.1 Pixel Array Structure

The new structure of TFT array is shown in Figure 2. It has the half the number of data lines and twice the number of gate lines compared to conventional one. Each data line has two pixels of the same polarity in the left at Nth gate line and right at (N+1)th gate line and this repeats till the end of the gate line. This arrangement not only reduces the power consumption using column inversion method but also eliminates the vertical crosstalk by using the pixel arrays similar to that of dot inversion pixel array. Furthermore, vertical flickering is also prevented.

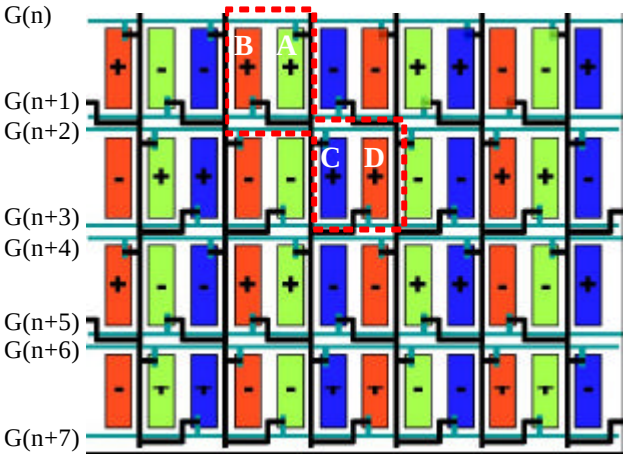

Figure 2. The TFT Array for Proposed Method

2.2 Driving Scheme

Such a TFT array structure can easily realize column inversion and applies pre-charge method to prevent reduced charging time due to the reduced number of data line. This is explained in Figure 3, which shows the incoming gate pulse with twice the charging time interval. In this way, instead of charging only one line at a time, two line could be charged simultaneously. At each time interval, one line that was charged at previous time interval is charged again. Therefore, the actual charging time does not decrease and good image quality remains.

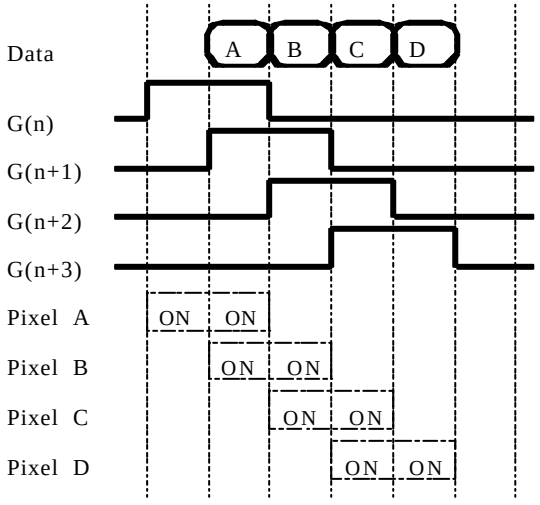

Figure 3. Gate Driving Signals for Proposed Method

2.3 Integrated a-Si Gate Driver

Gate drivers are integrated into amorphous silicon glass substrate to eliminate the need for gate driver IC's [4]. Figure 4 reveals the block diagram of an integrated gate driver.

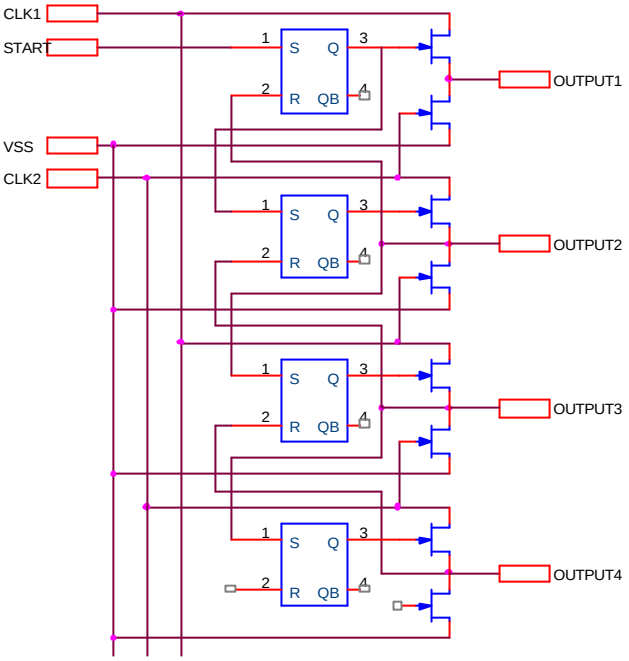

Figure 4. The Block Diagram of the Gate Driver

Gate driver circuit consists of two power clocks, one power supply and one input power signal. There are total number of 1,600 gate drivers and one more additional driver in the end. Each driver stage contains shift register and the output buffer that passes the carry onto the next gate driver and activates the connected gate line. The layout of integrated gate driver is shown in Figure 5. Additional circuit was designed to compensate for the voltage threshold shift of those transistors that perform important function. At the last driver state, the noise amplification at each stage is compensated.

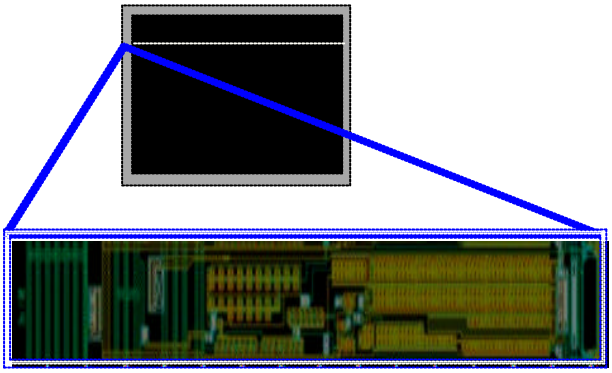

Figure 5. The Layout Gate Driver Circuit

2.4 Cost Estimation

Table 1 is the break-down of the total circuit cost. For conventional LCD modules, data driver IC and gate driver IC take up 44% and 19% respectively. Previous data line sharing technique reduced the data lines to half but doubled the gate lines, eventually leading to no cost reduction. This new technique, however, reduces the number of data driver IC, which is fabricated from expensive material, and at the same time eliminates the external gate lines leading to almost 41% of cost reduction in terms of circuit cost.

Table 1. The Circuit Cost Breakdown of LCD Module

Item	Conventional	Proposed Method	Remark
Data Driver IC	44%	22%	-22%
Gate Driver IC	19%	0%	-19%
Timing Controller	3.5%	3.5%	-
PCB	18%	18%	-
Peripheral	15.5%	15.5%	-
Total	100%	59%	-41%

2.4 Power Estimation

Generally, data line sharing technique requires twice the number of gate lines and increases the power consumption by about 20% with dot inversion method. In order to decrease the increase in power consumption, therefore column inversion method is strongly recommended. Table 2 shows the comparison between conventional and new panels in terms of power consumption. For all test patterns, lower power consumptions were measured. For the most power-consuming pattern, sub-dot pattern, a new module applying proposed technique produced 1.329W compared to 1.403W of conventional one. It's 5.3% reduction in power consumption.

Table 2. The Power Consumption of LCD Module

Item	Conventional	Proposed Method	Remark
White pattern	1.123W (340.5mA)	1.095W (332mA)	
Black pattern	1.239W (375.5mA)	1.043W (316mA)	
SubDot pattern	1.403W (424mA)	1.329W (403mA)	-5.3%

3. Impact

The proposed method was designed and tested using 15.4 inch WXGA TFT-LCD panel. Table 3 shows the performance comparison between the conventional and the proposed method. Figure 6 shows the pictures of the conventional panel and the one manufactured using the proposed technique. Compared to 10 data driver IC's and 3 gate driver IC's that conventional panel requires, only 5 data driver IC's are needed. This reduces the total circuit cost by more than 41% with 5.3% reduction in power consumption. Image quality as good as conventional panel was kept without crosstalk and vertical flickering. Furthermore, the integration of the gate driver circuits in the amorphous silicon glass substrate demonstrates the feasibility of circuit integration, which amorphous silicon have been thought to be inadequate for long time. This technique will lead to more compact and more cost-effective TFT-LCD panels that would quickly become widespread in LCD industries.

Table 3. 15.4inch LCD Specification

Item	Conventional	Proposed Method
Display Size	15.4 Inch Diagonal	15.4 Inch Diagonal
Dot Clock	68.9MHz	68.9MHz
Number of Data/Gate Line	1280/800	640/1600
Power Consumption	1.403W	1.329W
Image Quality	Good	Good

4. References

[1] M. Sakamoto, S. Okutani, K. Koga, H. Hada, and S. Ohi, "Half-Column-Line Driving Method for Low-Power and Low-Cost TFT-LCDs" SID'97, pp. 387-390, 1997.

[2] Sung, Y.-C., Choi, B.-D., and Kwon, O.-K. " A shared column-line driving method for high pixel density". SID'02, pp. 913-915, 2002.

[3] Kodate, M., and Kanazaki, E., "Pixel-level data-line multiplexing for low cost/high resolution AMLCDs". SID'02, pp. 1009-1011, 2002.

[4] R.G. Stewart, "Circuit Design for a-Si AMLCDs with Integrated Drivers," SID'95, pp. 89-92, 1995..

Figure 6. Conventional 15.4 inch module(left) and Proposed 15.4 inch Module(right)