Improvement of the On-Current for the Symmetric Dual-Gate TFT Structure by Floating N+ Channel

Dae Yeon LEE
Dept. of Electrical Engineering, Korea University, 5-Ka, Anam-Dong, Sungbuk-Gu, SEOUL 136-701, KOREA
Sang Jun Hwang, Sang won Park, Man Young SUNG*
Dept. of Electrical Engineering, Korea University, 5-Ka, Anam-Dong, Sungbuk-Gu, SEOUL 136-701, KOREA
- *E-mail : semicad@korea.ac.kr
- Phone : +82-2-3290-3214

Abstract
We have simulated a symmetric dual-gate TFT which has triple floating n+ channel to improve the on-current of the dual-gate TFT. We achieved a low hole concentration at the source and channel junction causes the improvement the potential barrier so that we observed the reduction of the kink-effect. In this paper, we observed the reduction of the kink-effect compared with the conventional single-gate TFT and the improvement of the on-current compared with the conventional dual-gate TFT.

1. Introduction
In general TFTs, the output characteristics exhibit an anomalous increases in the saturation current, often calls kink-effect. The kink-effect cause an increases of the output conductance of the drain current in the saturation region.[1] It causes several undesirable effects in the electrical characteristics. To overcome this kink-effect, the dual-gate structure has been used but drawback of the this structure is a low on-current.[2] So we proposed a new dual-gate structure which has triple floating n+ channel in the total channel region. We observed a reduction of the kink-effect as well as the conventional dual-gate structure. In addition the on-current of the proposed dual-gate structure is enhanced 80% compared with the conventional dual-gate structure.

2. Simulation
We simulated the device by 2-D numerical simulation program ISE-TCAD. The single crystal silicon active layer 400 nm in thickness on 100 nm oxide was bonded by anodic bonding method at 380 ℃, 700 V in a EBS-200A. The floating n+ channel were doped by ion-implanting Phosphorus at 100 keV with dose of 2×10^{5} /cm^{3}, activated by annealing at 500 ℃ in nitrogen. The source and drain were doped by implanting Phosphorus at 130 keV with dose of 4×10^{5} /cm^{3}, activated by an anneal 550 ℃ in nitrogen. A 150 nm gate oxide was deposited by LPCVD and A 700 nm Molybdenum was subsequently deposited by sputtering method for the source and drain contact. Fig. 1 shows a cross section of the proposed dual-gate structure.

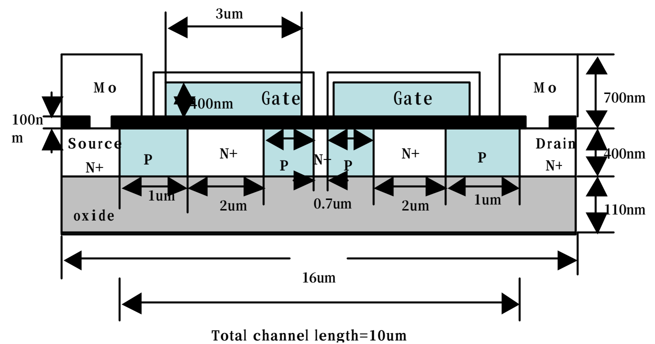

Figure 1. The symmetric dual-gate TFT with triple floating n+ channel.

3. Results
In this paper, we observed electrical characteristics for the proposed TFT at variable gate and drain voltage. Moreover we achieved the low hole concentration, low electric field in the channel region while the enhanced potential barrier at a source junction. Lowering the electric field and the hole concentration result show in drastic reduction of kink-effect. In addition this proposed structure allows an increase of the on-current by triple floating n+ channel compared with the conventional dual-gate TFTs.

3.1 The I-V output characteristics
Fig. 2 shows the drain current – drain voltage output characteristics for the conventional single and dual gate TFT and the proposed dual gate TFT at V_G=7 V

and V_D=12 V. The drain voltage range was from 0.1 V to 12 V and gate voltage is fixed at 7 V. All of the TFTs channel length was 10 um and gate width was 20 um. The saturation drain current of the conventional single-gate TFT increases in the saturation region continuously. This results from the kink-effect, which causes the premature breakdown in the TFTs.[3] The conventional dual-gate structure shows a stable drain current in the saturation region but on-current is so low due to lowering the electric field at the drain junction. The proposed dual-gate structure exhibits a enhanced on-current compared with the conventional dual-gate TFT. The on-current of the proposed dual-gate structure is 0.9 mA while that of the conventional dual-gate structure is 0.5 mA at a 12 V drain and a 7 V gate voltage. This result shows a 80% enhancement in on-current due to the channel resistance reduction by triple n+ channel.

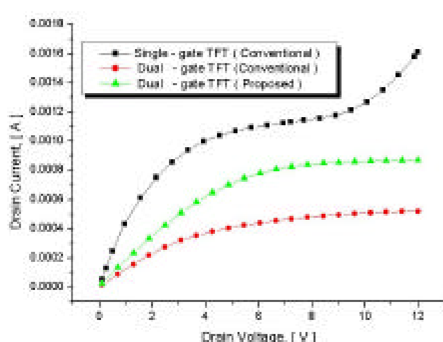

Figure 2. The I-V characteristics for conventional single-gate, dual-gate, and proposed dual-gate TFT. (V_D=12 V, V_G= 7 V)

3.2 The Output Conductance

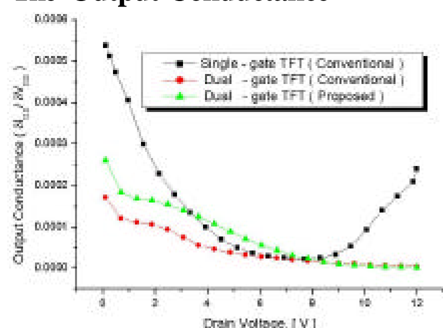

Figure 3. The output conductance (V_D=12 V, V_G=7V)

Fig. 3 shows the output conductance of the conventional single-gate, the conventional dual-gate and the proposed dual-gate TFT. The output conductance which increases continuously in the saturation region means that the drain current increases and consequently causes the premature breakdown in the TFTs. The kink effect of the proposed dual gate TFT is drastically reduced as well as that of the conventional dual gate TFT as shown Fig 3.

3.3 The Electrostatic Potential Barrier

The injection of electrons to the channel from the source contact cause the lowering the potential barrier and consequently cause an increase of the drain current in the saturation region. Fig. 4 shows the potential barrier of the conventional single, the dual - gate TFT and the proposed dual-gate TFT. The potential barrier of the proposed dual-gate TFT enhanced while that of the conventional TFTs. Fig. 5 shows the zoom in of the source and channel junction. The potential of the conventional single-gate is under 0.5 V and that of the conventional dual-gate is about 2.3 V and that of the proposed dual-gate is about 2.7 V at a 5 um point. This result induces by lowering the hole concentration in the channel region.

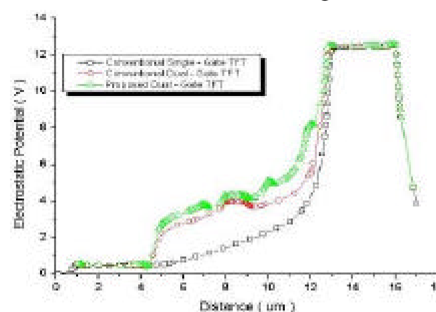

Figure 4. The potential barrier.(V)(V_D=12V,V_G=7V)

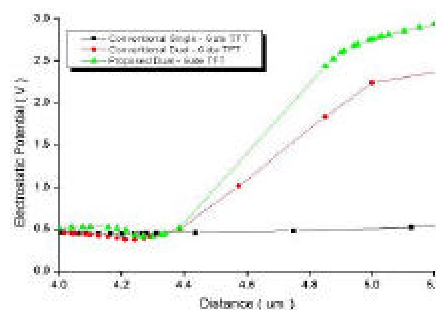

Figure 5. The zoom in between source and channel junction

3.4 The Hole Concentration

Fig. 6 shows the hole concentration of the conventional single gate, the conventional dual gate TFT and the proposed dual gate TFT. The hole concentration is an important parameter in kink-effect analysis. In the conventional single gate TFTs, the

holes generated by impact ionization at the drain junction can flow toward the source contact in the back-channel region and cause a potential barrier lowering at the source junction(PBT action).[4-5] The hole concentration of the proposed dual gate TFT at the source contact starting point(4.3 um) is very low because of the recombination between the floating n+ channels and holes. This result displays the prevention of the hole injection to the source contact so that the preclusion of the injection of electron to the channel as shown Fig 6. Fig. 7 shows the zoom in of the source and channel junction region. The hole concentration of the conventional single gate TFT is about 10^{17} /cm^3 and that of the conventional dual gate TFT is about 10^0~10^1 /cm^3 and that of the proposed dual gate TFT is about 10^{-1}~10^{-2} /cm^3.

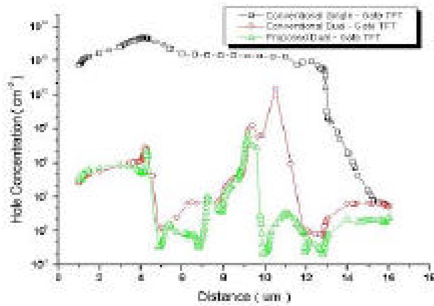

Figure 6. The hole concentration (V_D=12 V, V_G=7V)

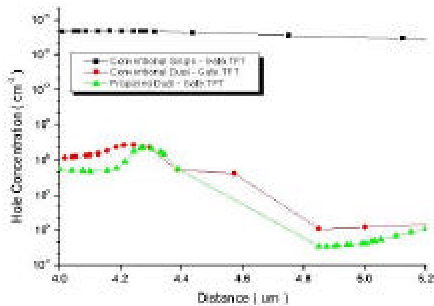

Figure 7. The zoom in between source and channel Junction

4. Conclusion

The new dual-gate TFT structure with triple floating n+ channels allowed us to reduce of kink-effect drastically. We confirmed the stable output conductance by the reduction of the hole concentration so that induced reduction of kink-effect. Moreover the triple floating n+ channels caused the reduction of electric field at the drain/channel contact region to delay the premature breakdown. In addition, this structure showed that the improvement of on-current compared to conventional dual-gate TFT. On-current showed a 80 % enhancement compared with the conventional dual gate TFT. Finally, the simulated single crystal silicon dual-gate TFT structure appears very effective in limiting kink-effect. In addition, if doping element changes to the As or An instead of Phosphorus, we expect a more smaller channel length size of the TFT.

5. References

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