

Fabrication of MILC poly-Si TFT using scanning-RTA and light absorption layer

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Abstract

We investigated light absorption layer effect on metal-induced lateral crystallization (MILC) growth rate and MILC thin films transistors (TFTs). As annealing method, we used scanning-rapid thermal annealing (RTA).

MILC growth rate which was crystallized by light absorption layer and using scanning-RTA was 3 times than normal MILC which was without light absorption layer growth rate. Also we compared MILC TFTs characteristics which were combined to light absorption layer with conventional MILC TFTs. After scanning-RTA process, MILC-TFTs which were with light absorption layer were superior to conventional MILC-TFTs.

With this new MILC-TFTs structure, we could reduced crystallization time and obtain good electrical properties.

1. Introduction

These days, low-temperature crystallization for producing large-grained poly Silicon (poly-Si) films has been studied extensively. They have technological importance in large-area microelectronic applications such as active matrix liquid crystal displays (AMLCDs) or organic light emission diode (OLED) displays for the fabrication of thin films transistors (TFTs). Because poly-Si TFTs have great quality such as higher current, faster switching rate and smaller cell structure than amorphous silicon thin films transistors (a-Si TFTs). Moreover, poly-Si TFTs are desirable as they can enable integration of various driver components directly onto the substrate.

For fabrication of poly-Si TFTs at low temperature, metal-induced lateral crystallization (MILC) method is performed.¹ It has high potential to be used for application using glass substrate without causing much damage on it. However, this process takes long time under the furnace annealing to crystallize silicon.

In order to improve production efficiency, it is essential to develop continuous annealing process^{2, 3}, so we use scanning-rapid thermal annealing (RTA) process. Amorphous silicon film was radiated by halogen lamp selectively^{4,5} and absorbed the emitted light. And then it transformed into crystalline silicon by MILC.

2. Experiments

We fabricated thin film transistors using scanning-RTA. To enhance absorbing efficiency, the light-absorption layer was inserted to TFT structure. Using them, we could achieve a more efficient productivity and better TFT performance.

2.1 Light absorption layer

Figure 1 shows the schematic diagram of sample structure.

3000 Å of SiO₂ layer was deposited on Corning 1737 glass substrate for a buffer layer. And then 600 Å of a-Si thin film was deposited by low pressure chemical vapor deposition (LPCVD). It was patterned by photolithography and reactive ion etching (RIE). 2000 Å of gate oxide was prepared by plasma enhanced chemical vapor deposition (PECVD) at 420 °C. 1000 Å of MoW for gate metal and 100 Å of Ni were deposited using sputtering system respectively. The source and drain regions were doped using Ion Mass Doping System (IMDS) of boron. Also, 4000 Å of SiO₂ for insulating layer and 1000 Å of MoW light-absorption layer were sequentially deposited on it, respectively. Finally, 1000 Å of SiO₂ capping layer was deposited by PECVD on it.

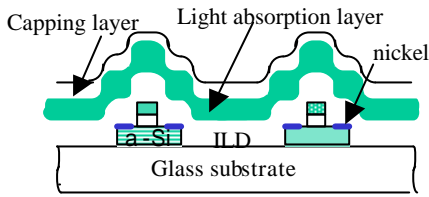


Figure 1. Schematic diagram of sample structure

2.2 Scanning-RTA process

In our study, this new structure was annealed the scanning-RTA.

Figure 2. shows the schematic diagram of the scanning-RTA system. Scanning speed was 1mm/sec and halogen lamp power was 2000 watt. Post hydrogen annealing for a passivation was performed in furnace for 1 hour at 450 .

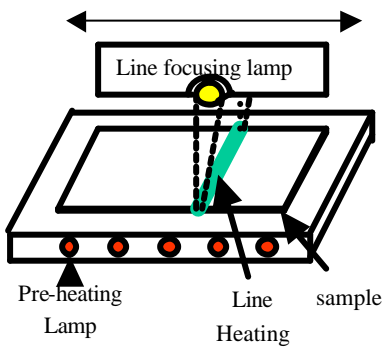


Figure 2. schematic diagram of scanning-RTA

3. Results

The MILC growth rate was 2 um per a scanning under this condition. In the contrast, the MILC growth rate in a conventional furnace annealing was 4um/h in hydrogen ambient at 570 .

Figure 3. and Table 1. show the transfer characteristics and the electrical properties of ptype poly-Si TFT between scanning-RTA crystallization and conventional furnace crystallization. The electrical properties such as threshold voltage (Vth), on-current (Ion), off-current (Ioff), on-off current ratio (Ion/Ioff) and mobility (μ) were better than those of conventional MILC TFTs. Also physical damages on the glass substrate were not observed such as bending and wrapping.

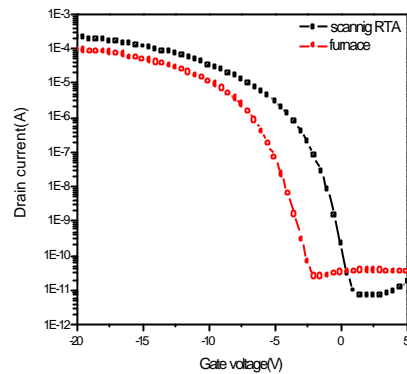


Figure 3. Transfer characteristics of pTFT between scanning-RTA crystallization and conventional furnace crystallization; W/L=10/10, drain voltage = 10.1V

	Scanning-RTA	Furnace
Vth (V)	-4	-6.5
Ion (A)	4.0E-4	1.3E-4
Ioff (A)	6.9E-12	2.4E-11
Ion/Ioff	5.8E7	5.4E6
μ (cm ² /Vs)	-60	-40

Table 1. Electrical properties characteristics of pTFT between scanning-RTA crystallization and conventional furnace crystallization

4. Summary

In this study, without any physical damage on glass substrate, poly silicon thin film transistor was successfully fabricated by our new process that was used scanning-rapid thermal annealing and light absorption layer.

With this new process, the crystallization rate was increased and the electrical properties of thin film transistor were improved dramatically.

5. Acknowledgements

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6. References

[1] S. W. Lee and S. K. Joo, IEEE Electron Device Lett., 17(4), 160 (1996)

- [2] L.K. Lam, S.K. Chen, Appl. Phys. Lett, 74 (13), 1866 (1999)
- [3] M. Bonnel, N. Duhamel, L.Haji and J. Stoemenos, IEEE Transactions on electron devices lett. 14 (12), 551 (1993)
- [4] H.S. Kim, J.G. couillard, and D.G Ast, Appl.Phys. Lett, 72(7), p.803 (1998)
- [5] Ichio Yudasaka and Hiroyuki Ohshima, Jpn. J. Appl. Phys. Vol.33, pp.1256-1260, Part 1.No. 3A (1994)