New Doping Process for low temperature poly silicon TFT

Kyungmin Park*, Chungi You[1], Chiwoo Kim[2]
LTPS Team, LCD Business, Samsung Electronics Co. San24, Nongseo-ri, Giheung-eup, Yongin-si, 449-711, Korea
E-mail : km.park@samsung.com, TEL : 82-31-209-9894

Abstract
We report the self-aligned low temperature poly silicon (LTPS) TFT process using simple doping process. In conventional LTPS-TFT, the Lightly Doped Drain (LDD) doping and source/drain doping are processed separately by aligning the gate with the source and drain during the gate lithography step. This new process not only fabricates fully self-aligned low temperature poly silicon TFTs with symmetric LDD structure but also simplifies the process flow with combined source/drain doping and LDD doping in one step. LDD doping process can be achieved using only source/drain doping process according to the new structure.
In this paper, the TFT characteristics of NMOS and PMOS using the new doping process will be discussed.

1. Introduction
Low temperature polycrystalline silicon (LTPS) technology has been the most promising TFTs. LTPS thin film transistors will offer performance and cost advantages in active matrix liquid crystal displays (AMLCD) due to its high carrier mobility compared to a-Si TFTs [1]. High carrier mobility of LTPS TFT enables to reduce the size of the TFT resulting in integrating driver ICs. However, the off-state leakage current of LTPS TFT is higher than a-Si TFT due to the high electric field near the drain junction and grain boundary trap state density. In the LTPS TFT, off set structure and Lightly Doped Drain (LDD) structure are employed to suppress off-state leakage current [2-3].

In conventional LTPS TFT, the LDD doping and source/drain doping are processed separately by using another mask or aligning the gate with the source and drain during the gate lithography step. However, this manufacturing process makes complicate the LTPS process and high the production cost. This new doping process not only fabricates fully self-aligned LTPS TFTs with symmetric LDD structure but also simplifies the process flow with combined source/drain doping and LDD doping in one step. LDD doping process can be achieved using only source/drain doping process owing to the new structure.

2. TFT fabrication
In this experiment, top-gate and lightly doped drain (LDD) n-channel and p-channel TFTs (N-TFT and P-TFT) were employed. First of all, 500Å a-Si and 5000 Å silicon oxide buffer layer were deposited by Plasma enhanced chemical vapor deposition (PECVD) on the glass substrate sequentially. After a-Si film deposition, sequential lateral solidification (SLS) was carried out to produce high quality polycrystalline silicon film. Gate Insulator film was deposited by PECVD after active islands patterned, and then channel doping was employed for controlling of threshold voltage(Vth). Gate Insulator film was employed dual layer of silicon oxide and silicon nitride for one step doping structure. For gate electrode, 3000 Å AlNd alloy was used. After the gate etching process, the silicon nitride film in the gate insulator film was removed by dry etching process. The different etching selectivity of silicon oxide and silicon nitride completely got rid of silicon nitride leaving behind silicon oxide layer. And then, photo resist was removed. Next, N+ or P+ source/drain doping was processed to form source/drain regions and LDD region at the same time. (P+ or N+ doping was performed to make the N-TFT or P-TFT respectively) The dual layer of silicon oxide and silicon nitride defined LDD region and the Source/Drain regions were formed through the single layer of silicon oxide. Etching of contact holes were followed by inter-layer dielectrics film deposition. MoW Metal layer was employed for source/drain connection. Fig.1 shows the schematic cross-sectional view of one step doping structure, so it can simplify

[1] If necessary, you may place some address information in a footnote, or in a named section at the end of your paper.

the doping process compared to conventional fabrication method.

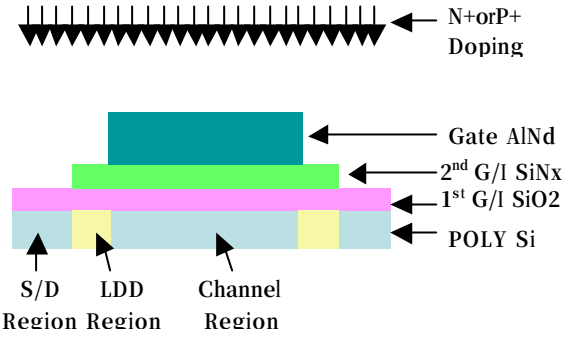

Fig 1. The schematic cross-sectional view of one step doping structure

3. Results and discussion

3.1 N-TFT characteristics

Fig.2 is the SEM image of one step doping structure after etching silicon nitride layer of Gate insulator. It was observed that the LDD region is about 0.7~0.8μm.

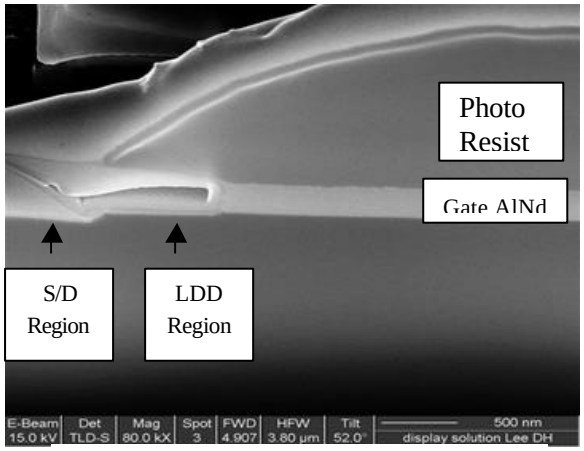

Fig 2. The SEM Image of one step doping structure.

The thickness of silicon oxide and silicon nitride of gate insulator was approximately 400Å and 400Å respectively, and then the different N+ source/drain doping energy was applied. The doping energies were 50KeV, 40KeV, 30KeV, 27KeV, 25KeV, 23KeV, and 20KeV, and the doping dose was fixed to 8E14 to make sure of the doping energy effect. Fig.3 shows the Vgs-Ids characteristics of N-TFT according to the doping energy. When the doping energy was 50KeV, TFT was not operating at all which meant source/drain doping energy was so high that source/drain regions were not activated by furnace annealing. When the doping energy was between 25KeV and 40KeV, off-state leakage current was increased by the decrease of gate voltage (Vgs is in off-state region). This was due to the heavily doped LDD region by high doping energy. When the doping energies were 23KeV and 20KeV, off-state leakage current was sustained with the voltage. This showed LDD region was well defined at the doping energies of 20KeV and 23KeV.

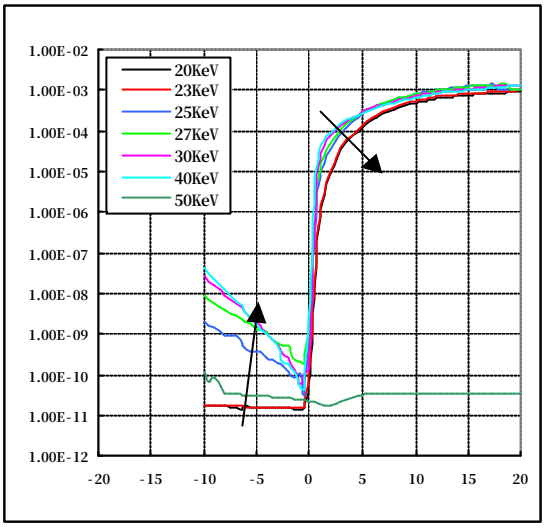

Fig 3. Vgs-Ids characteristics of N-TFT under source/drain doping energy

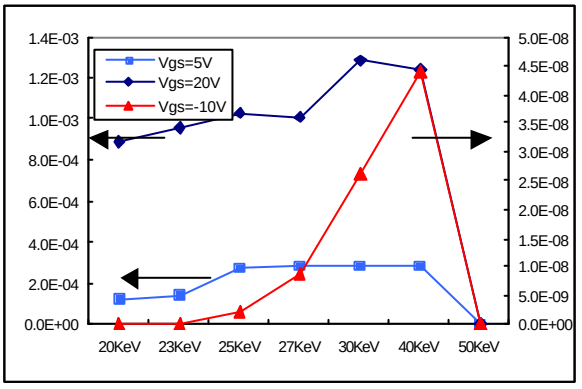

Fig 4. Off-state leakage current at Vgs=-10V and on current at Vgs=5V, 20V under source/drain doping energy.

Fig.4 shows the off-state leakage current and on-current according to the source/drain doping energy at various Vgs voltage. As you can see from Fig.4, both the off-state leakage current at Vgs=-10V and on

current at Vgs=5V and 20V were reduced as the doping energy was decreased.

We investigated the influence of the doping energy on the n-type Si/metal contact resistance. Fig.5 shows the change of the n-type Si/metal contact resistance owing to doping energy. When the doping energy was 20KeV and 40KeV, n-type Si/Metal Contact resistance was higher than that of other doping conditions. The optimum doping energy for n-channel TFT using one step doping process was found out to be 23KeV considering off-state leakage current, on current, and n-type Si/metal contact resistance .

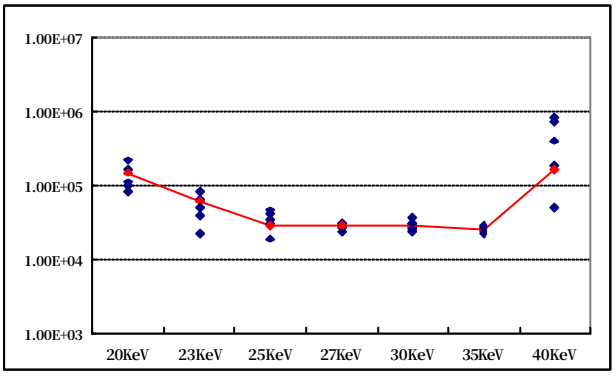

Fig.5 the change of the n-type Si/metal contact doping energy

3.2 P-TFT characteristics

The doping energy and the dose was fixed to 20KeV and 8E14 in the case of P-TFT, and the thickness of silicon oxide and silicon nitride for gate insulator was split to 400Å/400Å, 400Å/800Å, and 700Å/700Å. Fig.5 shows the Vgs-Ids characteristics of P-TFT according to the thickness of gate insulator. When the silicon oxide and silicon nitride thickness of gate insulator was 400Å/400Å, the off-state leakage current was increased by decreasing of gate voltage. This phenomenon was same as N-TFT characteristics. When the silicon oxide and silicon nitride thickness of gate insulator was 400Å/800Å, the off-state leakage current was lower than the leakage current of 400Å/400Å. However, the off-state leakage current still increased as Vgs increased. (Vgs was off state voltage)

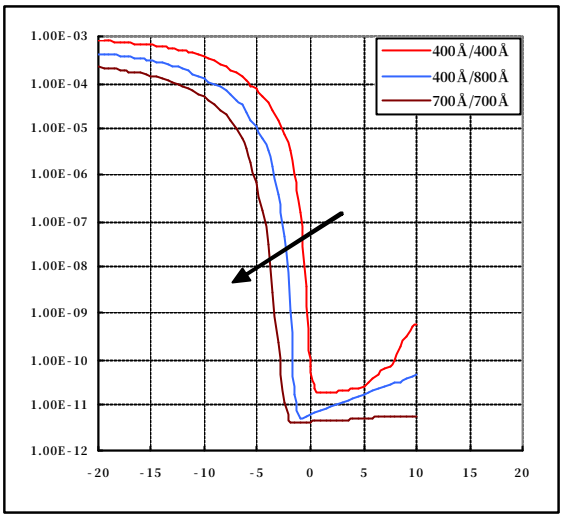

Fig.6 Vgs-Ids characteristics of P-TFT according to the thickness of gate insulator.

When the silicon oxide and silicon nitride thickness of gate insulator was 700Å/700Å, the off-state leakage current was sustained to sub pA. LDD region for one step doping structure in case of P-TFT could be achieved by controlling the thickness of silicon oxide and silicon nitride. It was important to control the total thickness of gate insulator in the LDD region for off-state leakage current. However, threshold voltage (Vth) shifted negatively depending on the thickness of silicon oxide and silicon nitride in gate insulators at the same channel doping condition.

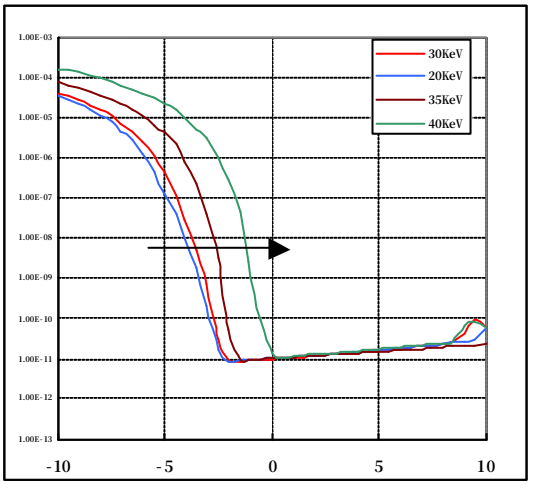

Fig.7 The positive shift of Vth according to the channel doping energy.

The fixed charge and energy band gap difference between silicon oxide and silicon nitride gave rise to the negative Vth shift.[4] We evaluated the channel doping condition to control the Vth shift. Fig.6 shows the positive shift of Vth according to the channel doping energy at the gate insulator thickness of 700Å/700Å. As you can see from Fig.6, Vth moves positive as the doping energy increases. The optimum thickness of silicon oxide and silicon nitride for gate insulator in case of p-channel TFT using one step doping process was found out to be 700Å/700Å considering off-state leakage current and on current. The channel doping energy of 40KeV should be performed to control the Vth shift.

4. Conclusion

We applied 400Å/400Å for the thickness of silicon oxide and silicon nitride for the gate insulator of N-TFT, and experimented different thickness of silicon oxide and silicon nitride for the gate insulator of P-TFT. We achieved the good characteristics of N-TFT and P-TFT using one step doping process. It can be achieved by controlling the doping energy in case of N-TFT, and by changing the thickness of silicon oxide and silicon nitride in the gate insulator in case of P-TFT.

5. Acknowledgements

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6. References

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