A Low-Power Gate Driver IC for TFT-LCD Application

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Abstract
A low-power gate driver IC, which can be used for TFT-LCD application, is proposed. The short-circuit current of the output buffer is greatly reduced. An experimental prototype gate driver implemented in a 0.35-mm CMOS technology demonstrates that the power reduction of 16 % is obtained.

1. Introduction

With the evolution of compact, light-weighted, low-power and high quality displays, there is a big demand to develop a low-power dissipation Thin-Film-Transistor Liquid-Crystal Display (TFT-LCD) driver [1-2]. An TFT-LCD driver is generally composed of gate drivers, source drivers, a timing controller, and a reference source [3]. A gate driver IC comprises shift registers, level shifters, and output buffers [4]. Since hundreds of output buffers are built in a single gate-driver IC and the output buffers drive hundreds of highly capacitive gate lines with high voltage drive, the power dissipated in the output buffers are dominated in the gate-driver IC. The conventional output buffer utilizes the taper buffer, which is consisted of several inverters. However, the short-circuit current of the last stage of the inverter chain will be very large. This increases the power consumption. In this work, a new output buffer, in which the short-circuit current is greatly reduced, is proposed and demonstrated.

2. Proposed Gate Driver

The implemented block diagram of the gate-driver IC is shown in Figure 1, in which the shift registers are used to generate a series of positive pulses, the level shifters shift the positive pulses to higher levels, and the output buffers are used to drive the highly capacitive gate lines. The schematic of the proposed output buffer is shown in Figure 2. The feedback transistors M3 and M4 are used to reduce the short-circuit current. When the input is in the low state, the output is low and M4 is turned off. As the input is raised to a high level, M4 will not be turned on immediately. This reduces the circuit-short current. Similarly, the short-circuit current of the input transient from high to low level will also be greatly reduced due to the existence of M3. The transistors M3 and M4 will limit the output voltage range. However, this limitation is solved by another feedback circuit, which is circled by the dashed line in the figure.

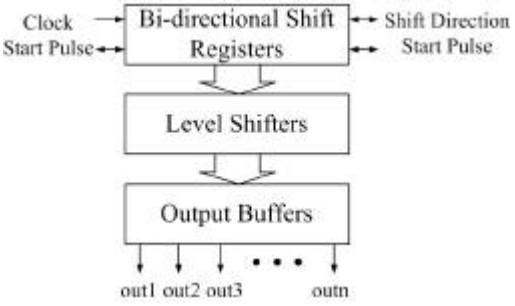

Figure 1 The implemented block diagram of the gate-driver IC.

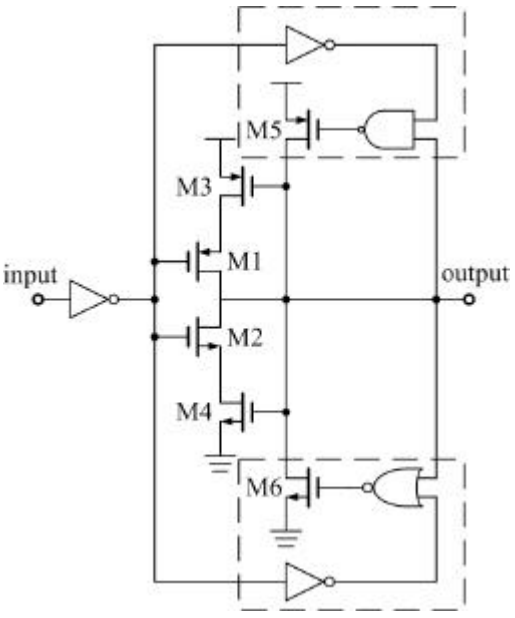

Figure 2 The schematic of the proposed output buffer.

3. Experimental Results

A 26-channel gate-driver IC, which utilized the proposed output buffer, was fabricated using a 0.35-μm CMOS technology. The photograph of the prototype gate-driver IC is shown in Figure 3. The proposed gate-driver IC is measured under 1 KΩ resistor and 250-pF capacitive load with a power supply of 3.3 V and 5 V. The power supply of 3.3 V is used in the digital circuits and 5 V is for the level shifters and output buffers. The measured output waveforms for two neighboring channels under 2 MHz are shown in Figure 4. The performance summary is shown in Table I.

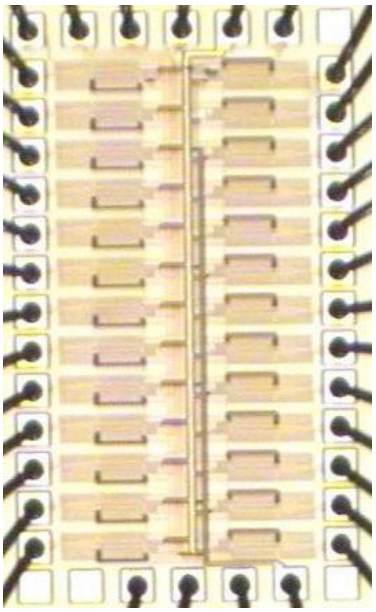

Figure 3 The photograph of the prototype gate-driver IC.

4. Conclusions

In this work, a low-power gate-driver IC is proposed. The short-circuit current of the output buffer is greatly reduced. An experimental prototype gate-driver IC implemented in a 0.35-μm CMOS technology demonstrates that the power consumption is only 30 mW for driving a 1 KΩ resistor and 250-pF capacitive gate line. The power reduction of 16 % is obtained.

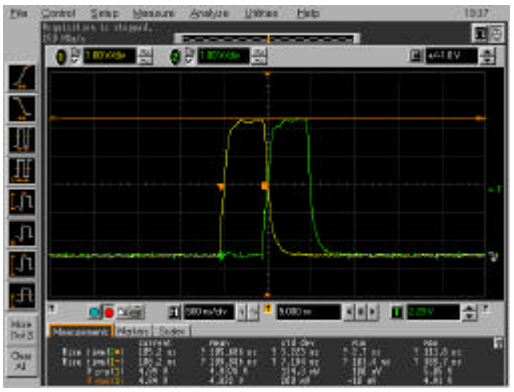

Figure 4 The measured output waveforms for two neighboring channels under 2 MHz.

Table I Performance summary.

VDD (digital circuit)	3.3 V
VDD (output buffer)	5 V
Frequency	2 MHz
Power Consumption	30 mW
Power saving	16 %
Rising time	105 ns
Falling time	110 ns

5. References

[1] Chih-Wen Lu and Chung Len Lee "A Low Power High Speed Class-AB Buffer Amplifier for Flat Panel Display Application", *IEEE Transactions on VLSI Systems*, Vol 10, No. 2, pp. 163-168, April 2002.

[2] Pang-Cheng Yu and Jiin-Chuan Wu, "A Class-B Output Buffer for Flat-Panel-Display Column Driver," IEEE Journal of Solid-State Circuits, Vol. 34, No.1, Jan. pp. 116-119, 1999.

[3] Jong-Seok Kim, Deog-Kyoon Jeong, and Gyudong Kim, "A Multi-Level Multi-Phase Charge-Recycling Method for Low-Power AMLCD Column Drivers," IEEE Journal of Solid-State Circuits, Vol. 35, No. 1, January, pp. 74-84, 2000.

[4] http://www.ti.com/.