Current Saturation Improvement of Poly-Si TFTs for Analog Circuit Integration

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Abstract
New poly-Si TFTs have been proposed and fabricated in order to increases the output channel resistance (r_o). The counter-doped (p^+) source is tied to the n^+ source and is extended into the channel region so that it employs the reverse bias depletion in the channel. As V_{DS} is increased, the depletion width is increased and the effective channel width is reduced. Therefore, the output current saturates well and the r_o is increased successfully. The proposed CMOS devices may improve the amplifier gain of data driver in active-matrix displays
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1. Introduction

Polycrystalline silicon thin film transistors (Poly-Si TFTs), of which the mobility and on-current is rather large, has attracted a considerable attention for AMLCDs and AMOLEDs [1-2]. Recently, the panel integration using the poly-Si TFTs is going to realize by high-performance transistors and the circuit design developments. However, the kink current due to an inherent floating body structure of thin film transistor is a critical issue [3]. Also, the channel resistance is not practically too large so that the saturation current would be rather increased as V_{DS} is increased. The output resistance should be increased in order to achieve high-performance poly-Si driver circuits such as a high gain amplifier for an analog buffer, a stable current source [4].

The purpose of our work is to propose the poly-Si TFTs employing reverse bias depletion for kink suppression and highly current saturation. The counter-doped (p+) source is embedded into the channel region so that p+n junction is formed in the channel region. The p+ terminal can collect the hole currents due to the electron-hole generation so that the kinks are suppressed and the output resistance would be increased. Also, as V_{DS} is increased, the channel width is effectively controlled by reverse biased p+n depletion. Therefore, the output resistance (r_o) is increased and the saturation slope ($1/r_o$) is successfully decreased. The proposed CMOS poly-Si TFTs may be employed to the analog circuitry such as differential amplifiers, analog buffers, current source.

2. Proposed Device Physics

The proposed poly-Si TFT employing counter-doped source is shown in Figure 1a. In the n-type poly-SI TFTs, the counter-doped p+ source is tied to n+ source and prolonged into the channel region. Therefore, p^+n junction is formed in the channel region when the n-channel is formed in the surface of channel by $V_{GS} > V_{TH}$. In the experiment, the width and length of the channel is W = 15μm and L = 20μm, repectively. The width and length of prolonged p+ source are Wp = 4μm and Lp = 15μm. The proposed structure employs n-type and p-type self-align doping by the gate and is compatible to the conventional CMOS process.

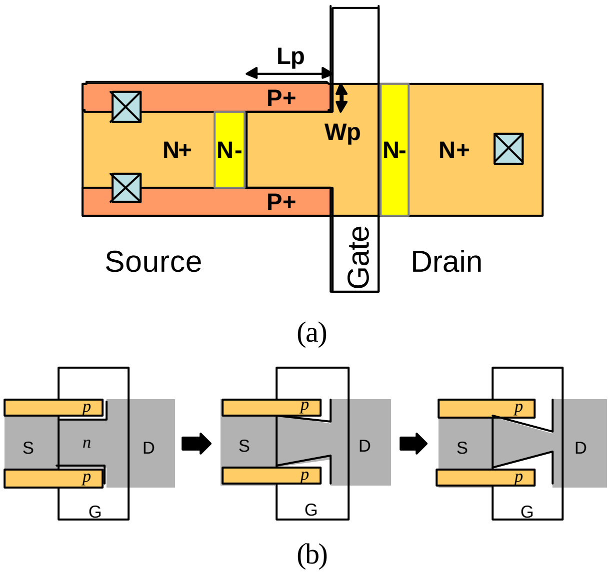

Figure 1. (a) The proposed poly-Si TFT employing the counter-doped p+ region (b) The effective channel width reduction according to V_{DS} increase

The extended p+ source is constituted in the n-type channel region in order to achieve a reverse bias depletion. At once, V_{GS} is biased larger than V_{TH}, the transistor turns on and the inversion layer (n-channel) is formed in the channel region. Since the p+ body is tied to the n+ source and biased lower than the channel potential, there will be created the depletion between the extended p+ body and the n-channel current path. When V_{DS} is increased, the channel potential is also increased and the reverse bias (V_R) of p^+n depletion is increased and the depletion width (W_{depl}) is increased as follows [5],

$$x_n = \sqrt{\frac{2\varepsilon_s (V_{bi} + V_R)}{e} \frac{N_a}{N_d} \left[\frac{1}{N_a + N_d}\right]}$$

Here, it is noted that the depletion width is functional to the V_R and the V_R is also functional to the V_{DS}. The counter-doped source is highly p^+ doped compared with the created n-channel concentration in the undoped channel so that almost depletion width may belongs to the n-channel region ($W_{depl} = x_p + x_n \cong x_n$).

In the depletion region, the current path is not allowed so that the channel width is reduced effectively ($W_{eff} = W - 2x_n$). For $V_R = 1.5V$, the x_n is calculated by 0.55µm and $W_{eff} = 7 - 1.1 = 5.9$µm. Therefore, I_{DS} current equations of the conventional and the proposed poly-Si TFTs may be described by the equation as follows,

$$I_{DS} = \frac{W_{eff}\,\mu C_{ox}}{2L} (V_{GS} - V_{TH})^2 [1 + \lambda(V_{DS} - V_{DS.SAT})]$$

$$= \frac{(W - 2x_n)\,\mu C_{ox}}{2L} (V_{GS} - V_{TH})^2 [1 + \lambda(V_{DS} - V_{DS.SAT})]$$

$$= \frac{W\mu C_{ox}}{2L} (V_{GS} - V_{TH})^2 [1 + \lambda(V_{DS} - V_{DS.SAT})][1 - \alpha\sqrt{f(V_{DS})}\,]$$

Here, the lamda (λ) is denoted by the current saturation factor [6], which is obtained empirically due to the kink effect and the low output resistance of poly-Si TFTs. In the proposed devices, the current increase according to V_{DS} may be suppressed by the reduced channel width as illustrated in Figure 1b. In our proposed device, the channel length and width may be scaled and reduced for various applications. If the dimensions of TFTs are small, the effective width reduction is dominant and the current saturation would be improved.

3. Experimental Results

The fabrication process is compatible with the conventional CMOS LTPS (450°C) process and no additional mask step is required. Figure 2 shows the photography of the fabricated poly-Si TFT of 20µm channel length. The crystallization of a-Si film and the source and drain activation was performed by XeCl (λ=308nm) excimer laser. The p+ body terminal is formed compatibly to the p+ source and drain process of pMOS.

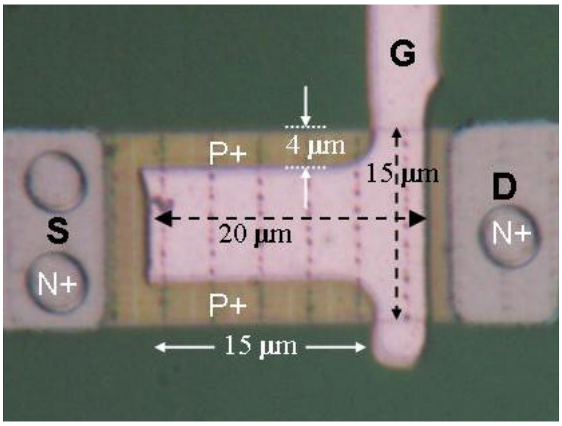

Figure 2. The photography of the faricated poly-Si TFT employing the extended counter-doped body terminals in the channel

The measured output characteristics of the conventional and the proposed poly-Si TFT is shown in Figure 3. The channel width and length of the conventional TFT is 15µm and 20µm, respectively. In the proprosed one, the width at the drain is also 15µm, while the width is narrrowed to 7µm at the source due to the extended p+ bodies. The output saturation current of conventional TFT is increased as V_{DS} is increased, while that of proposed TFT is suppressed successfully. It is because the counter-doped p+ node induces a reverse bias depletion into the n-channel region and the current path is narrowered as V_{DS} increased. The output resistance (r_o), which is inversely proportional to the saturation slope ($1/r_o = \partial V_{DS} / \partial I_{DS}$), is r_o = 1.67 V/µA @V_{GS}=9V and V_{DS}=6~10V, and is increased by 3.3 times larger than the conventional one (0.5 V/µA). The kink current is also suppressed and the kink starting points are retarded, which may be contributed by the hole collection of counter-doped p^+ bodies [7].

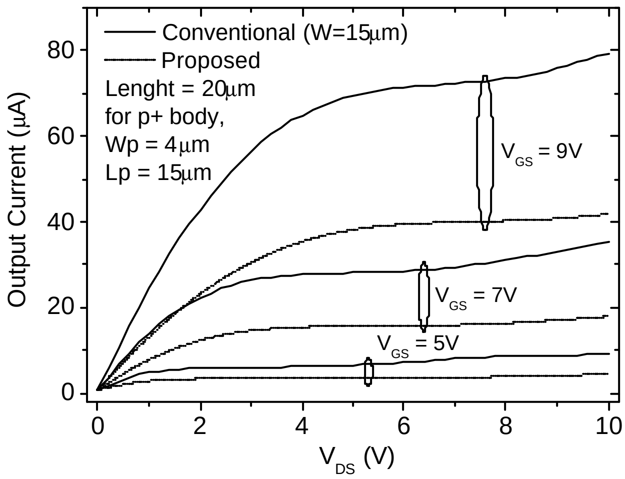

Figure 3. The measured output current of the fabricated poly-Si TFTs

4. Analog Circuit Design

4.1 Differential Amplifier

The large r_o is important to achieve the analog circuits of the data driver employing poly-Si TFTs. In the differential amplifier (Figure 4), the gain (A_v) is dependent on the transconductance (g_m) and output resistance (r_o) as follows [8],

$$A_v = -g_m \cdot (r_{oN} \,||\, r_{oP})$$

$$g_m = \sqrt{(2 \cdot \mu_n \cdot Cox \cdot (W/L) \cdot I_D)}$$

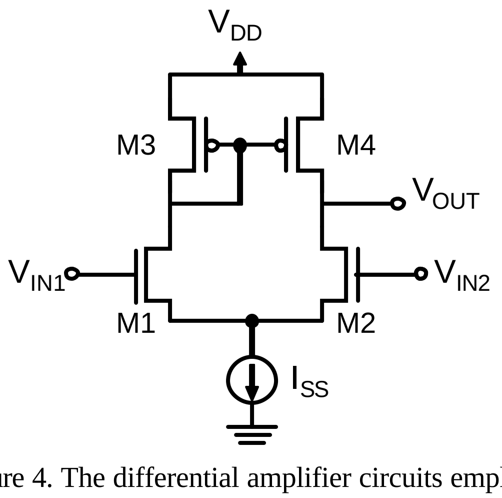

Figure 4. The differential amplifier circuits employing the extended counter-doped body in M1 and M2 transistors

In order to increase the gain, the g_m as well as r_o should be increased. However, when the channel length is decreased and g_m is increased, the r_o would be decreased typically. In the proposed device, the r_o is rather larger compared with the conventional one so that the gain is increased for the same channel length.

In Figure 3, the transconductances of the conventional and the proposed device at V_{DS}=3V and V_{GS}=5V are calculated. Since the current level in the saturation regime is 6.054μA and 3.425μA,

$$g_{mconv} = \sqrt{(2 \cdot 179 \cdot 3.5 \cdot 10^{-8} \cdot (15/20) \cdot .6.054 \cdot 10^{-6})}$$
$$= 7.5\ (\mu A/V)$$

$$g_{mpropsd} = \sqrt{(2 \cdot 179 \cdot 3.5 \cdot 10^{-8} \cdot (7/20) \cdot .3.425 \cdot 10^{-6})}$$
$$= 3.8\ (\mu A/V)$$

In the proposed, it is difficult to obtain the exact g_m value because the width dimension varies in the channel (7μm to 15μm in Figure 2). Thus, we assume and calculated the width = 7μm in convenience. And the output resistance (r_{oN}) is calculated at V_{GS}=5V and V_{DS}=3~8V,

$$r_{oN.conv} = (8-3) / (8.558 - 6.054) = 2\ M\Omega$$

$$r_{oN.propsd} = (8-3) / (3.866 - 3.425) = 11.3\ M\Omega$$

In order to examine the amplifier gain, we assume $r_{oP} = 4 \cdot r_{oN.conv} = 8M\Omega$. Then the gain will be,

$$A_{v.conv} = -7.5\mu \cdot (2M \,||\, 8M) = -12$$

$$A_{v.propsd} = -3.8\mu \cdot (11.3M \,||\, 8M) = -17.8$$

Therefore, the gain using the proposed device is rather large compared with the conventional case. The gain of amplifier varies with the current level of the current source I_{SS}, the input voltages, the dimensions of the transistors. Therefore, the numerical comparison of the gain values (17.8 by 12) does not conclude a considerable improvement exactly. However, the overall gain of multi-stage amplifier is multiplied by each gain of stages so that it may depend on the starting gain value considerably. The r_{oP} is higher than r_{oN} typically and the gain may be maximized up to $A_v \sim -g_m \cdot r_{oN}$ when $r_{oN} \ll r_{oP}$. The increase of gain means the decrease of the offset deviation when we design the unit-gain buffer.

4.2 AMOLED Pixel Circuits

Recently, poly-Si TFT is considered for the pixel driving elements of active-matrix organic light emitting diode (AMOLED) display. For OLED current driving TFT, a kink current reduction with high output resistance (r_o) is required for an analog-voltage controlled transsistor in the saturation regime. The OLED current may vary by the V_{DS} variation and it also varies when the threshold voltage of OLED is non-uniformly shifted and degraded as shown in Figure 5. Therefore, kink-free output characteristics become more important in AMOLED pixel TFTs for controllable OLED current. The improved saturation characteristics may be immune against the OLED current variation due to the threshold voltage degradation of OLED as well as kink characteristics.

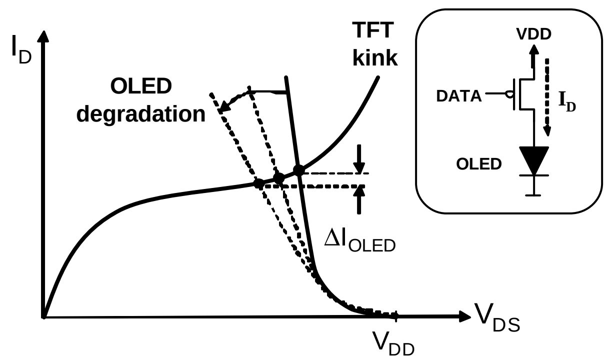

Figure 5. AMOLED pixel circuit and the OLED current variation by the output characteristics of OLED and TFT

The proposed extended counter-doped terminal poly-Si TFTs reduce kink current so that they are applicable to AMOLED pixel circuit. The brightness of OLED luminance is sensitive to the current level within ~1µA. In other words, the gray scale may vary by the small current no more than 20nA difference. Therefore, the pixel circuit employing the proposed device would exhibit rather uniform brightness. Although the pixel circuit is designed by CMOS process rather than nMOS or pMOS only, the approach for reduction of the control signal lines is reported now [10].

5. Conclusions

The current saturation of poly-Si TFTs should be improved in order to achieve the high-performance poly-Si analog circuit integration. The proposed poly-Si TFT employs the extended counter-doped body terminals in order to increase the output resistance. As the drain bias is increased, it controls the effective channel width by the reverse bias depletion in the channel so that the currenti is well-saturated. And the counter-doped body does collect the generated holes due to the impact ionization, thus suppresses the kink current. The device fabrication is also compatible with the conventional CMOS LTPS process without any additional mask. The output characteristics of the proposed TFT will improve the performances of analog circuits such as an increase of the amplifier gain and the fine control of OLED current driving.

6. References

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