2.8 inch QVGA System On Panel LCD Employing Advanced CMOS LTPS Technology

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Abstract

A 2.8 inch fully integrated SOP employing a high performance LTPS CMOS TFT technology has been developed for mobile display applications. The LCD module is directly interfaced with 3V 6-bit RGB source via timing control circuitry. The integrated data driver comprises a 6-bit hybrid type DAC with low power analog buffer.

1. Introduction

LTPS (Low Temperature Polycrystalline Silicon) technology has numerous advantages over a-Si (Amorphous Silicon) counterpart in mobile applications, resulting in compact, high resolution and low power displays.[1] LTPS technology leads to a future concept of SOP (System On Panel), where all the electronic components related to the display can be interfaced inside the panel itself via large-scale integration.[2] SOP technology will bring forth a new class of display applications due to their highly productive and reliable module configurations.[3] The compactness and simplicity of the SOP module will give higher degree of freedom to the system designers, which will broaden the applications in mobile communications and multimedia.[4]

However, the current LTPS technologies do not fulfill the rather strict requirements for realizing the SOP.[5] TFT device requires high mobility; over 200cm^2/Vsec, lower threshold voltage; under 1V, not to mention the good reliability under high-speed operation. The device characteristics greatly dependent on the material properties of the LTPS film itself and the insulators vicinity of the conducting channel.

In order to improve the device characteristics of LTPS TFTs, an advanced process technology has been developed. We have focused our work on optimizing the crystallization methodology and surface treatment of the active film. This paper also reports a 2.8-inch QVGA AMLCD panel with low power drive circuits employing the proposed CMOS LTPS technology.

2. Experiment : Advanced LTPS Device

The buffer insulator comprises SiNx and SiO_2 double layer deposited sequentially using PECVD. SiNx buffer inclusion enhances the stability of the flatband voltage, as an effect of forming a blocking layer for impurity diffusion from the glass substrate . After depositing the a-Si:H active layer, P- ion doping is performed for counter-doping the channel of n-TFT. Then, laser induced crystallization is performed. Average of 2um poly-Si grain is sequentially grown by scanning an array of microstrip excimer laser beam with energy density over 400mJ/cm^2. Then, the glass is dipped in a diluted fluoric acid (HF) solution to remove the residual impurities on the active layer surface. Gate insulator is deposited, followed by gate metallization. P^+ / N^+ ion doping is performed, followed by N^- ion doping to form LDD (Lightly Doped Drain) structure. The TFT fabrication is followed by metallization and passivation.

The transfer characteristics of an n-channel LDD and a p-channel devices with W/L = 4um/4um are shown in Figure 1. and Table 1. The n-channel device has 1.5um lightly doped region in drain. The device performance is much enhanced compared to those of the conventional ELA devices, and the period of the crystallization process is reduced by 60%.

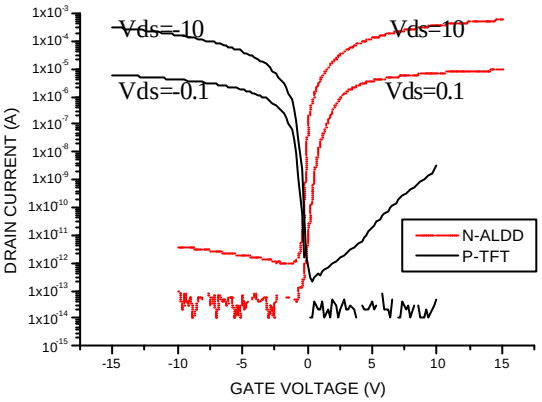

Figure 1. Characteristics of n-LDD, p-TFT fabricated employing the advanced CMOS LTPS technology.

Table 1. Device characteristics of TFTs fabricated with advanced LTPS technology

Device	Field effect mobility	Threshold voltage	Sub-threshold factor	Leakage current
P-TFT	110 cm^2/Vsec	-0.81V	0.19 V/dec	-29 pA
N-ALDD	260 cm^2/Vsec	0.82V	0.24 V/dec	2.3 pA
N-LDD	210 cm^2/Vsec	0.75V	0.24 V/dec	4.0 pA

3. Results and Discussion

3.1. Module

Figure 2 shows the schematic layout of the 2.8-inch SOP module. Source driver is integrated with 6-bit DAC (Digital-to-Analog Converter) with built-in gamma function. Timing controller is fully integrated to interface with 6-bit RGB digital source directly. Both gate and source driver has bi-directional scanning capability. The controller module is consisted of frame memory and power source. The controller and panel are interfaced with 90pin FPC.

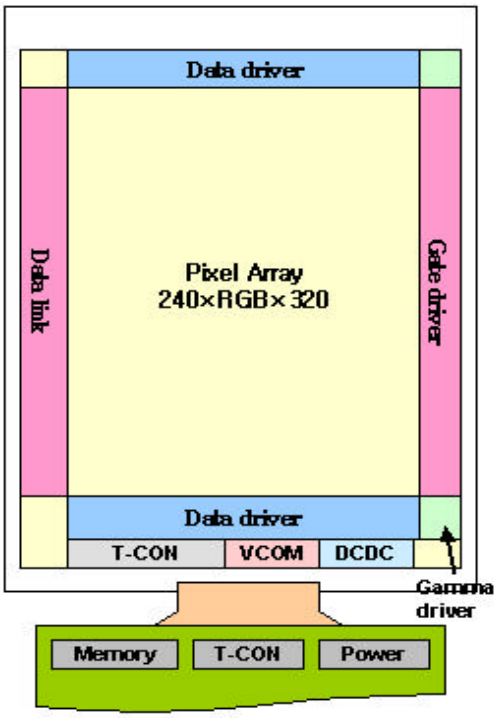

Figure 2. Schematic Diagram of 2.8 inch SOP module.

3.2. Driver and System Circuits

The gate driver is consisted of a shift-register, level-shifters and buffers, as shown in Figure 3. The data driver is consisted of a shift-register, level-shifters, latch arrays, 16-to-2 multiplexers for 4-bit resistive DACs, 2-bit capacitive DACs with analog buffers and RGB de-multiplexers, as shown in Figure 4. The peripheral circuit is consisted of a timing controller, a Vcom driver, a DC/DC converter, and a 16-level gamma voltage generator.

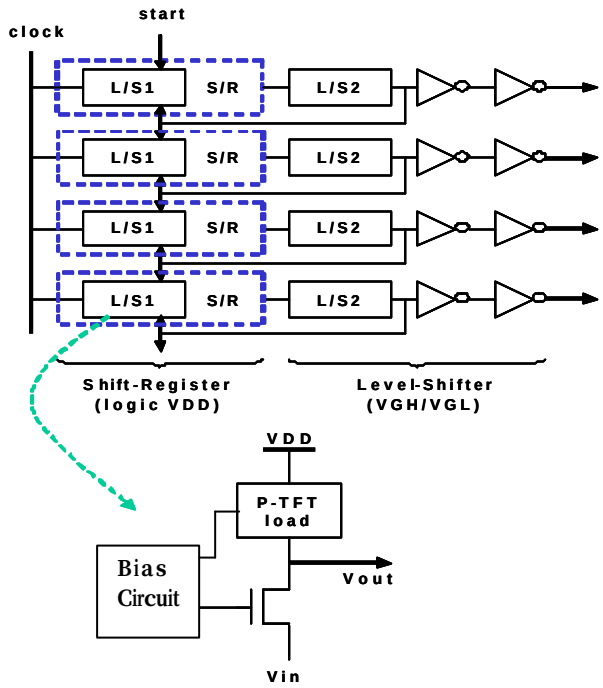

Figure 3. Integrated gate-driver circuitry with shift-register and selective level-shifter

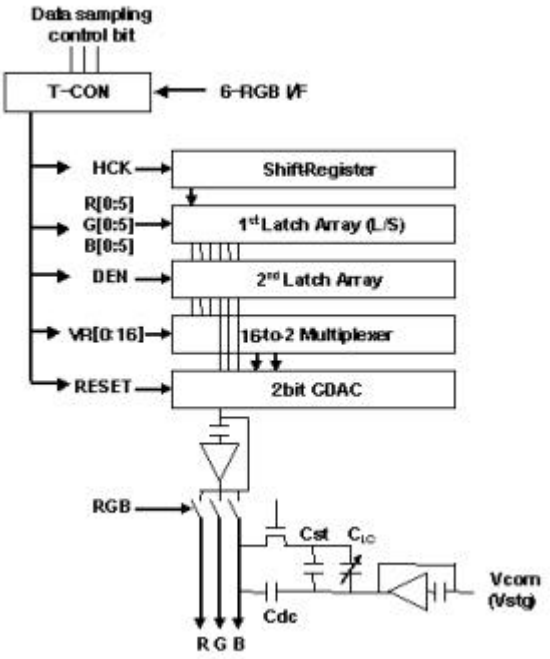

Figure 4. Integrated data-driver circuitry with 6-bit DAC and analog buffer.

The shift-registers for both gate and data drivers selectively amplify the input clock voltage, so that level-shifters operate only when necessary thus reduce power consumption. The level-shifter is a common-gate amplifier in a latch configuration; in order to increase the operation tolerance and reduce the thru current induced power consumption.

Low voltage digital video signal is amplified prior to being stored in the 6-bit line memory by single-input level-shifters. The 6-bit DAC is consisted of a 4-bit (MSB) resistive DAC (R-DAC) and a 2-bit (LSB) capacitive DAC (C-DAC). The C-DAC drives the panel data lines via an analog buffer, which is consisted of two stages of offset-compensated comparator and switched inverter. The VCOM circuitry is consisted of two blocks that take charge of high/low polarities. Each block includes an offset-compensated comparator and driving TFT. The charging of the node voltages between the LC (Liquid Crystal); one being the pixel (Vp), and the other being the common (Vcom) are complementary. Thus pixel node is charged with p-TFT and common node charged with n-TFT. Therefore, the voltage error, which may inherit from the overshoot phenomenon of uni-polar (or uni-directional) charging, is insignificant.

The specifications of the LCD panel are introduced in Table 2. The uniformity and reliability of the LTPS devices have been remarkably enhanced due to optimizing the processes related to the active film crystallization and the channel surface treatment. Channel doping also helps to stabilize the threshold characteristics of the n- and p-channel TFTs.

4. Conclusion

We have developed a 2.8 inch QVGA LCD panel with integrated drive circuits employing advanced CMOS LTPS process technology. The panel driving circuitry is fully integrated in order to realize a true SOP. 6-bit hybrid DAC and analog buffer operates under supply voltage less than 6 at 60Hz frame rate. The power dissipation is remarkably low due to suppression of the thru-currents in analog circuits.

Through this technology simplify module process, reduce the mobile-application panel cost.

5. References

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[2] M. Azami et al., *SID Digest*, p180, (1999).
[3] H. Otani et al., *SID Digest*, p467, (1998).

[4] K. Kanzaki, *Technical Digest of AMLCD*, p71, (2001).
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Table 2. Panel specifications

Feature	Spec.
Panel Dimension	72(H) x 48(W) mm
Diagonal	2.83 inch diagonal
Pixel Pitch	60 um x 180 um x 3 (141ppi)
Number of Pixels	240 x RGB x 320
Interface	RGB 6-bit
Display Type	Transmissive
Number of Terminals	90 pins
Interface Voltage	3.3V
Power Supply	10V / 6V / 0V
Function	Bi-directional scan : H / V