Low voltage stability of a-Si:H TFTs with SiN$_x$ dielectric films prepared by PECVD using Taguchi methods

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Abstract

The high stability of a-Si:H TFTs device is studied with different deposited conditions of SiN$_x$ films by PECVD. The process parameters of N$_2$, NH$_3$ gas flow rate, RF power, and pressures of hydrogenated amorphous silicon nitride are taken into account and analyzed by Taguchi experimental design method. The NH$_3$ gas flow rate and RF power are two major factors on the average threshold voltage and the a-SiN$_x$:H film's structure. The hydrogen contents in SiN$_x$ films were measured by FTIR using the related Si-H/N-H bonds ratio in a-SiN$_x$:H films. After the 330,000 sec gate bias stress is applied, the threshold voltages (V$_{th}$) shift less than 10%. This result indicates that the highly stable a-Si:H TFTs device can be fabricated with optimum gate SiN$_x$ insulator.

1. Introduction

The a-Si TFTs with a-SiN$_x$:H is widely adopted in AMLCD device. In fabrication process, the a-Si:H is deposited on top of a-SiN$_x$:H by PECVD to form a conducting channel between the silicon/insulator interface under gate bias voltage. Therefore, the characteristics of the thin film transistor device depend on the quality of the a-Si/a-SiN$_x$ interface, such as threshold voltage, electronic mobility, reliability and stability [1-4].

The a-SiN$_x$:H films deposited at 280°C using silane (SiH$_4$) and ammonia (NH$_3$) as the source gases by PECVD process have been developed in this study. The gate insulators of a-SiN$_x$ are prepared at various gas flow rates. Classical experimental design methods are too complex and not easy to carry out. Furthermore, a large number of experiments have to be done when the number of process parameters

increases. To solve this problem, Taguchi method [5] uses a special design of orthogonal arrays to study all of parameters with a minimum number of experiments. The experimental results are then converted into the signal-to-noise (S/N) ratio to determine the optimal conditions of experiment. Regardless of the category of the quality characteristic, the larger S/N ratio corresponds to the better characteristic quality. Therefore, the optimal level of the process parameters is the level with the highest S/N ratio. Usually, there are categories of quality characteristics in the analysis of the S/N ratio, which the nominal the best is chosen in this paper.

Nominal the best:

$$S/N = 10\log(\overline{y}^{\,2}/S^2)$$

The stressing experiments by using different stressing time with various gate voltages (V$_g$) at room temperature are used to evaluate the performance of devices. The previous results indicate that defect creation depends on the gate voltage, whereas charge injection strongly increases for gate-bias voltages above a critical value [6]. The gate insulator with different Si-H/N-H ratios will use to examine the stability of a-Si:H TFTs. The optimal process parameters for a-Si:H TFT device with smaller threshold voltage and less threshold voltage shift after the gate bias stress can be achieved in this study.

2. Experimental

Figure 1 is shown the cross sectional view of the inverted staggered a-Si:H TFT fabricated in this paper. The different preparing conditions of SiN$_x$ films were deposited by RF 13.56MHz plasma enhanced chemical vapor deposition using mixture

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gases of SiH_4, NH_3, N_2 and H_2 at 280°C. These samples were deposited a-SiN_x films at different process parameters of gases flow rate, RF power and pressure. The hydrogen contents in SiN_x films were determined by FTIR using the related Si-H/N-H intensity ratio in a-SiN_x:H films.

Four controllable parameters in Taguchi experimental design were identified, which are NH_3, N_2 gas flow rate, RF power and pressure, respectively, as listed in Table 1. This array is called "L_9" table. Orthogonal array is shown in Table 2. According to Table 2, we find the levels of the controllable factors that are the least influenced by the noise factors and that provide the maximum pull-off force.

The hydrogen contents in SiN_x films were measured by fourier transform infrared spectrometer (FTIR) used to obtain the related Si-H/N-H bonds ratio in a-SiN_x:H films. The device characteristics were measured by HP 4156B analyzer. The threshold voltage of various deposited parameters were extracted through Id-Vg curves and the stability properties were studied by the bias stress conditions of V_g=30V, V_d=V_s=0V under the 0sec, 1,000sec, 100,000sec and 330,000sec stressing time at room temperature, respectively.

3.   Results and Discussion

The graphs of the "marginal means" of each level on S/N ratio and average of threshold voltage are shown in Figure 2. Factors A (NH_3 gas flow rate) and B (N_2 gas flow rate) have larger effects on the S/N than do C (RF power) and D (pressure); factor A (NH_3 gas flow rate) and C (RF power) has larger effects on the $\bar{y}$ than do B and D. In terms of minimizing signal-to-noise ratio, the best-combined factors will be A3, B1, C1 and D2. In terms of minimizing the average threshold voltage $\bar{y}$, the best choices are A2, B1, C3, and D2. Beside on S/N, the factors affecting the dispersion are given in the decreasing order of importance: B (N_2 gas flow rate) > A (NH_3 gas flow rate) > C (RF power) ? D (pressure). The effects of control factors on $\bar{y}$ decrease in the order of A > C ? B ? D. Thus, the NH_3 gas flow rate (A) is the most important factor in maximizing signal-to-noise ratio (S/N) and minimizing the threshold voltage ($\bar{y}$) in deposited a-SiN_x:H films.

Figure 3 shows the Si-H/N-H bonds ratio in SiN_x films. To calculate the Si-H/N-H ratio from the FTIR measurement, the peaks around 2180cm^{-1} for Si-H

bond and 3340cm^{-1} for N-H bond were chosen from the FTIR spectra. An increasing power results in a decrease in Si-H and an increase N-H bond density. This indicates that the N-content and H-content both increase. The presence of Si-H bonds in a-SiN_x:H films can be explained by the contribution of silane radicals to the film growth. The higher power leads to dissociation of more NH_3 molecules, thus less Si-H bonds and more N and H in this film. According these results and analysis from Taguchi methods and Si-H/N-H bonds ratio, therefore, we choose that sample number #7 has the larger electronic mobility and less threshold voltage is the best-deposited parameter than the others.

The stress experiments of this sample by using various stressing time with gate voltage V_g=30V, drain and source voltages V_d=V_s=0V at room temperature are shown in Figure 4. The sample #1 is used as reference here for comparison. After the 330,000 sec gate bias stress time is applied, the threshold voltages (V_{th}) shift of sample number #1 and #7 about 20.93% and 6.78%, respectively, as shown in Figure 5. It indicates the #7 sample has higher stability with high field-effect mobility than that of #1 sample. These results confirm to S/N ratio that NH_3 gas flow rate and RF power are the most important factors on this study.

From the gate bias stress experiment, we observe the phenomenon of the threshold voltages that shift greater to left by increasing positive gate voltage after 1000sec stress time on sample #1, as shown in Figure 6. This charge current of TFT device included the electrons from the negative electrode and holes from the positive electrodes tunneling into the valence band in channel. The charges may either pass through the other electrode, causing leakage current, or they may become trapped in defect states deep within the band gap or dangle band of the dielectric layer. The detail of cross section of TFT device with electron conducting path is shown in Figure 7. It is evident the stress induced leakage current in TFT devices is due to electrons tunneling (charge injection) through stress-induced neutral traps in the channel between the semiconductor/insulator interfaces. The dielectric surface of SiN_x layer deposited by chemical vapor deposition method is the unstable condition with dangle-bands present. The present of contaminated dangle-bands can be forwarded to combine with electrons from fixed charge on the dielectric layer by

gate bias stressing that cause an I-V curve shift between the initial states and 1000sec stress time.

4. Conclusion

Using Taguchi method, it is found that the dominating factors for the stability of a-Si:H TFTs in PECVD process are N_2 gas flow rate, NH_3 gas flow rate, RF power, and pressure in descending importance on S/N ratio. The NH_3 gas flow rate and RF power are two major factors in minimizing the average threshold voltage. Under optimal parameters, the minimized threshold voltage shifts in a-Si:H for about 6.78% can be achieved after 330,000sec gate bias stress time. The stress induced leakage current indicates that some active traps are resulted from dangle-band between the a-Si/SiNₓ interfaces in the tunneling process and deactivated after 1000sec gate bias stress.

5. References

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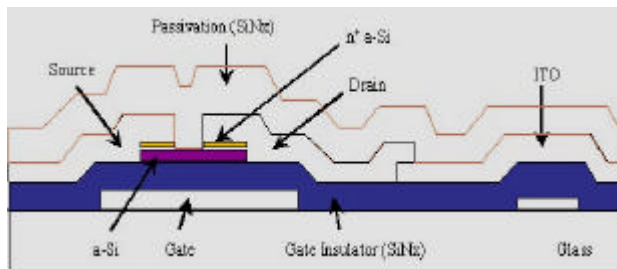[6] J. B. Choi, D. C. Yun, Y. I. Park and J. H. Kim, J. of Non-Cryst. Sol., 266-269, 1315 (2000).

Figure 1 The cross section view of a-Si:H TFT device.

Table 1 Factors and le vels design of the parameters.

Controllable Factors	Levels		
A NH₃ gas flow rate (sccm)	4700	7800	9400
B N₂ gas flow rate (sccm)	8900	10900	12900
C RF power (W)	500	650	800
D Pressure (mbar)	0.7	0.8	0.9

Table 2 L₉ orthogonal array for the dispersion factors.

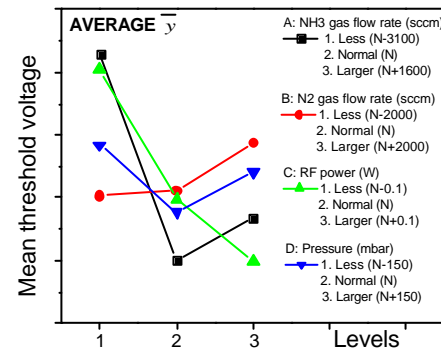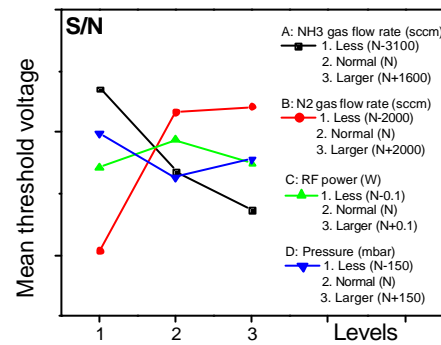| Experiments Sample No.	Factors			
	A	B	C	D
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

Figure 2 The effects of controllable factors on S/N ratio and average $\bar{y}$.
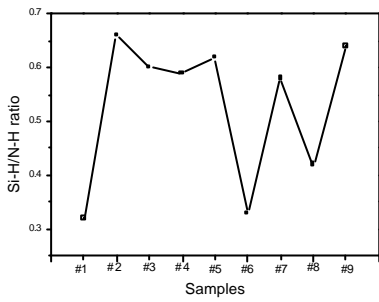
Figure 3 FTIR spectra of the Si-H/N-H bond ratio in various deposited parameters a-SiN$_x$:H films.
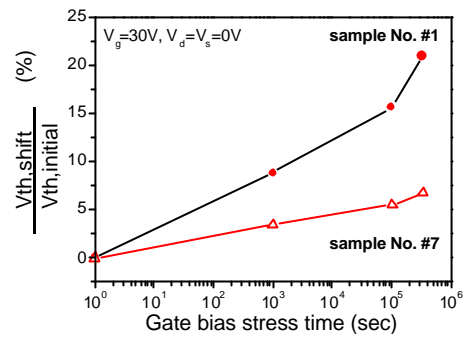

Figure 4 The Id-Vg curves of sample number #1 (a) and #7 (b) before/after different gate-bias stress time.

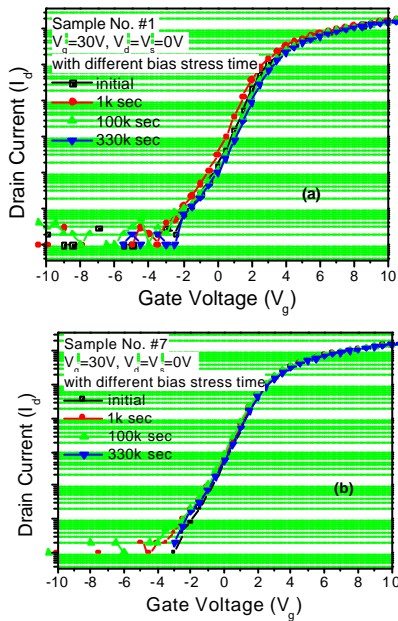Figure 5 The threshold voltage shift percentage of sample number # 1 and #7 at different gate bias stress time.
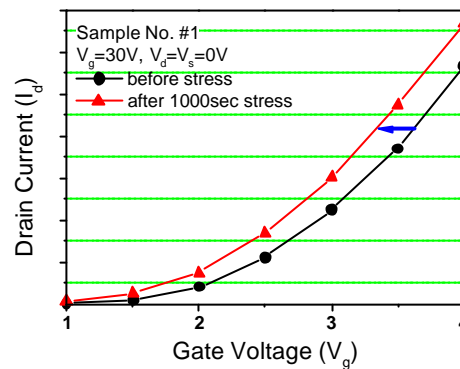

Figure 6 Drain current variations as a function of V$_g$ before and after stress on sample #1. The arrow is shown the stress induced leakage current.
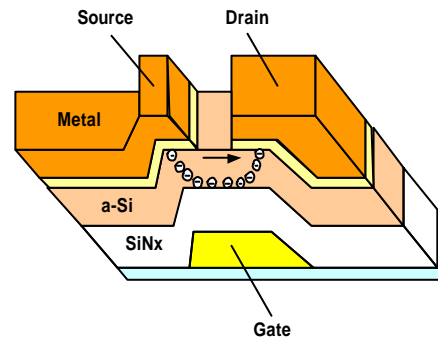

Figure 7 The detail of cross section of a-Si TFT device with electron conducting path.