Fabrication of Thin Film Transistor on PES substrate using Sequential Lateral Solidification Crystallized Poly-Si Films

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Abstract
Using optimized sputtering condition of a-Si and SiO_2 thin film, we can obtained the large grained poly-Si film on PES substrate. The gate dielectric grown by plasma enhanced atomic layer deposition, laser activation and organic interlayer dielectric material make TFTs on PES possible with mobility of 11 cm^2/Vs (nMOS) and 7 cm^2/Vs (pMOS).

1. Introduction
A plastic substrate is an obvious candidate for many flat-panel display applications where light weight, flexibility and robustness are required. Because most of the plastic substrates have a temperature-resistance up to 200°C, it is necessary to keep the processing temperature as low as possible. The interest in the low temperature poly-Si (LTPS) thin film transistor (TFT) stems from its much higher mobility than amorphous silicon (a-Si) TFT, which enables it to be used for the full integration of both the drive circuits and the pixel TFTs in a monolithic CMOS technology.

Amorphous silicon films that are deposited using plasma enhanced chemical vapor deposition (PECVD) at such a low temperature contain excessive hydrogen. Excimer laser annealing has been used in the crystallization of sputter deposited a-Si films. However, sequential lateral solidification (SLS) is the procedure of choice for the formation of high quality poly-Si films.

In this presentation, we report on the successful fabrication of thin film transistor using SLS crystallized poly-Si films on PES substrate.

2. Results and Discussion
The 80 nm a-Si film is deposited on 600nm SiO_2 buffer/polyethersulfone (PES) substrate in an RF magnetron sputtering system. The a-Si film was irradiated by excimer laser with a line/space = 2μm/4μm mask. The wavelength of the excimer laser light was 308 nm and the pulse duration was 25 ns.

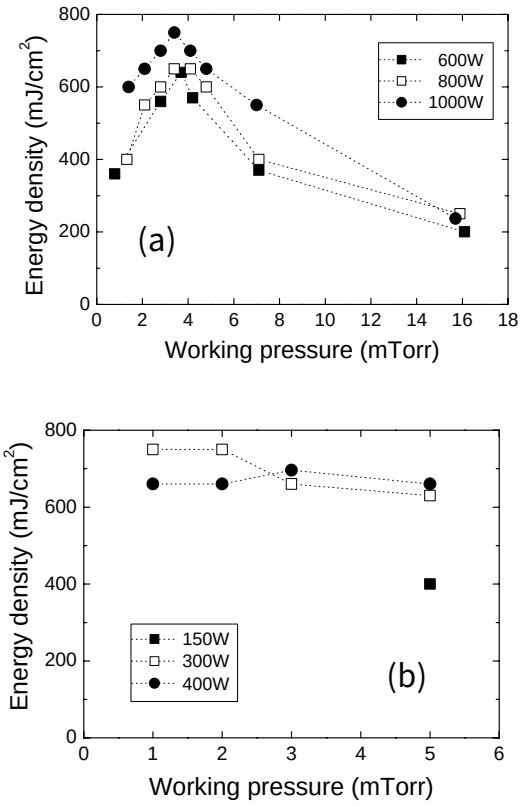

Fig. 1. Maximum laser energy density over which the a-Si film is damaged according to the sputtering condition of (a) amorphous Si and (b) SiO_2 thin film.

Figure 1 shows the maximum laser energy density over which the a-Si film is damaged according to the sputtering condition of (a) amorphous Si and (b) SiO_2 thin film. The optimum sputtering condition of a-Si thin film for highly resistant thin film is mainly influenced by the working pressure. But the sputtering

power has more influence at the sputtering condition of SiO_2 thin film. Low density SiO_2 film shows low melting temperature which inhibit the SLS process. We select the sputtering condition of a-Si film at 1kW, 3.6mTorr and of SiO_2 film at 300W, 1mTorr. The PES substrate is laminated on the glass wafer and the minimum sputtering power for SiO_2 film is chosen to reduce the film stress which induce the film's delamination from glass wafer.

Figure 2 shows the TEM image of poly-Si film with the super lateral grain growth.

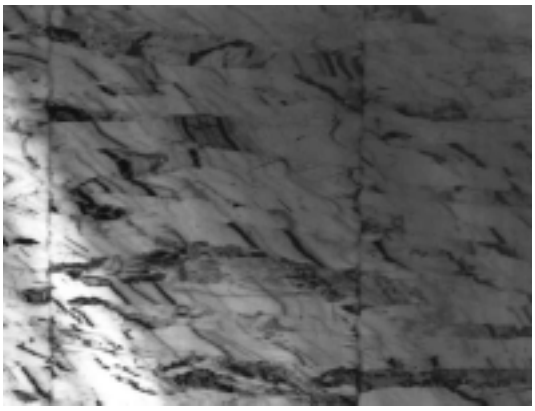

Fig. 2. TEM image of the successfully crystallized poly-Si thin film.

To obtain a high quality gate dielectric film, we formed 5 nm SiO_2 using an O_2 plasma treatment on the surface of the poly-Si film and then deposited 65 nm Al_2O_3 film containing nitrogen (< 1 %) by plasma enhanced atomic layer deposition at the temperature of 120°C [2]. The precursors of Al, O, and N are trimethylaluminum, O2, and N2, respectively.

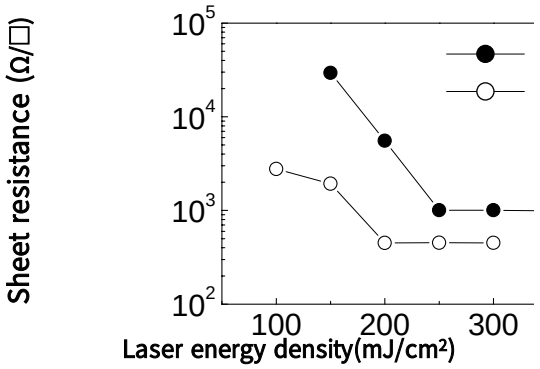

Fig. 3. Sheet resistance of the n+/p+ S/D sheet resistance with laser energy density

Following the gate dielectric formation, a Al gate electrode of 200 nm is formed by DC sputtering at room temperature because Cr gate is cracked during the thermal process. After the patterning of the gate electrode, the n+ and p+ source and drain (S/D) regions are formed by ion shower doping using PH_3/5keV and B_2H_6/20keV. Figure 3 shows the sheet resistance of the n+/p+ S/D with laser energy density. With laser energy of 300 mJ/cm^2, we obtained the S/D sheet resistance below 1 kΩ/□.

To reduce the stress on PES substrate, we used the organic interlayer dielectric material with 700 nm thickness which is baked at 120°C/2hours. Finally the contact hole opening is followed by 300 nm Al formation.

Figure 4 shows (a) the nMOS and (b) the pMOS transfer characteristics. The TFT of W/L = 30μm / 30μm on PES shows rather lower performance with mobility of 11 cm^2/Vs (nMOS) and 7 cm^2/Vs (pMOS) than that of TFT on Si wafer [2].

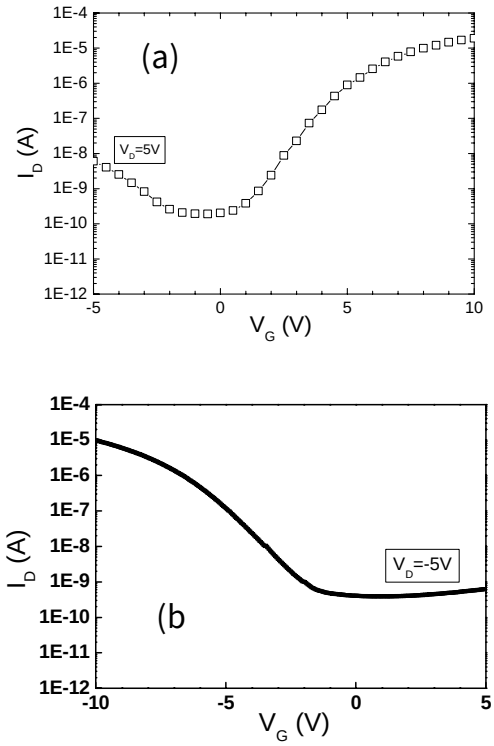

Fig. 4. Transfer characteristics of (a) nMOS and (b) pMOS.

3. Summary

Using optimized sputtering condition of a-Si and SiO_2 thin film, we can obtained the large grained poly-Si film on PES substrate. S/D Sheet resistance below 1 kΩ/□ is obtained by laser activation. TFTs on PES shows performance mobility of 11 cm^2/Vs (nMOS) and 7 cm^2/Vs (pMOS).

4. Acknowledgements

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5. References

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