플라즈마 디스플레이를 위한 서스테인 및 리셋 회로

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Sustain Driver and Reset Circuit for Plasma Display

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요 약

플라즈마 디스플레이를 위한 효율적인 서스테인 드라이버와 이를 리셋 회로와 결합시키는 유용한 결합 방법을 제시한다. 제안된 서스테인 드라이버는 외부 인덕터와 패널에 존재하는 기생 커패시터 간의 직렬공진 방식을 이용한다. 이 회로는 4개의 스위칭 소자, 인덕터, 전원 공급을 목적으로 하는 외부 커패시터로 구성된다. 기존의 방식과 비교하여 입력전원전압이 두 배가 되지만 스위칭 소자에 가해지는 전압스트레스는 기존의 값과 거의 동일하며, 입력 전압을 별도의 승압 없이 리셋 회로의 전원으로 사용할 수 있는 장점을 가진다. 이러한 회로적 구조는 서스테인 드라이버와 리셋 회로를 간단히 구성할 수 있다. 이론적 분석을 바탕으로 동작원리와 설계 예를 제시하며, 7.5 인치 AC PDP 패널을 이용한 실험을 통해 타당성을 검증한다.

ABSTRACT

An efficient sustain driver and a useful reset circuit composition technique are proposed for plasma display panel drive. The proposed sustain driver uses a series resonance between an external inductor and a panel to recover the energy dissipated by a capacitive displacement current of PDP. It consists of four switching devices, an inductor, and external capacitors, which supply sustain voltage sources. Although the amplitude of an input voltage source is twice as high as that of conventional sustain drivers, average voltage stress imposed on power switching devices is nearly same in their values. Moreover, the input voltage source can be directly applied for the use of a reset voltage source. Owing to this scheme, the proposed sustain driver and the embedded reset circuit have a simple configuration. The operational principle and design example are given with theoretical analyses. The validity of the proposed drive system is verified through experiments using a prototype equipped with a 7.5-inch-diagonal AC plasma display panel.

키워드

energy recovery, reset circuit, Plasma display panel (PDP), sustain driver.

Ⅰ. Introduction

In the display industry, an AC plasma display panel has been received a great consideration owing to its simplicity and durability. The operational principle of PDP is to make use of gas discharging generated ultraviolet ray to excite a visible ray emitting phosphor. However, the power consumption due to wall recombination of the electrons and ions in small cell makes the discharge less efficient than the well-known discharge lamps with a high lumen efficacy [1-3]. It is one of important reasons why PDP shows low efficiency compared to LCD (liquid crystal display) and CRT (cathode-ray tube) display methods. Generally, a PDP driven by an address-and-display-separated (ADS) method requires three special drivers, i.e., a reset circuit, an address driver, and sustain drivers.

As mentioned earlier, discharge of PDPs in the small cell has low luminous efficiency. If a sustain pulse frequency is increased in order to make it

high luminance, a circuit power loss will increase. For this reason, in order to reduce the power consumption of the whole display system, the drive circuit which can improve a circuit power loss is important the same with raising luminous efficiency. Although most power loss occur during the sustain discharge, the loss of sustain discharge can be minimized by an energy recovery circuit.

In this paper, a series resonant sustain driver and a useful reset circuit composition scheme are proposed. The proposed sustain driver uses a 2-level pulse to change voltage polarity across the panel and a series resonance between an inductor and an intrinsic panel capacitance to recover the energy from the panel. The proposed sustain driver consists of full-bridge inverter, an external inductor, and two external bulk capacitors. The amplitude of an input voltage source is twice as high as that of conventional sustain drivers. It is divided into two sub-voltage sources to supply sustain voltage to the proposed sustain circuit. And, the input voltage source is directly used as a reset voltage source. The validity of the proposed driver is verified through computer-aided simulations and experiments using a laboratory prototype. Simulation results of other sustain drivers using a 2-level sustaining pulse are given to assess the performance of the proposed driver.

II. Proposed sustain driver

Fig. 1 shows a configuration of the proposed sustin driver. It consists of four switching devices, an industor, two external bulk capacitors. The input voltage source (Vs) is separated into two sub-sources with the same value (Vs/2). Each sub-source is utilized for the use of voltage source of sustain drivers.

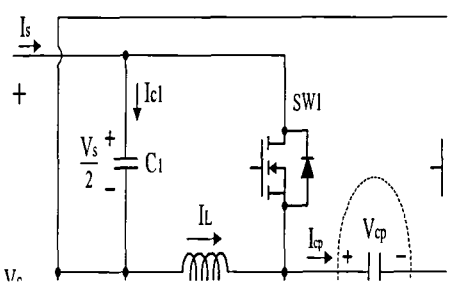

Fig. 1. Configuration of the proposed sustain driver

The principle of the energy recovery is to utilize a series resonance between an external inductor (L) and an intrinsic panel capacitance (Cp). A case where all switches are in a OFF state, voltage across the panel changes its polarity transferring energy from Cp to L and vice-versa. To shorten the transition period of panel voltage, the inductor stores sufficient energy from the external bulk capacitor (C1 or C2) in a prior stage.

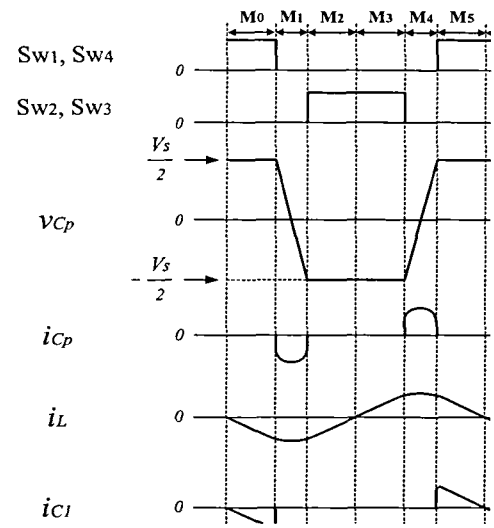

Fig. 2. Operational waveform

Fig. 2 shows operational waveform. We consider only two periods of the ADS driving method, i.e., the reset and sustain period. To simplify the circuit analysis, we ignore the effect of discharging current. We assume that the value of CP and the input voltage source (Vs) is constant. Voltage across C1 and C2 are exactly same in their values. All switching devices and components are ideal. The line inductance and resistance are ignored.

Mode 0 (t0-t1): At t=t0, Sw1 and Sw4 are conducting. Voltage across the panel maintains Vs/2. Current flowing through the panel is null. The inductor stores energy from the upper voltage source (C1).

Mode 1 (t1-t2): At t=t1, Sw1 and Sw4 are turned off at the same time while Dsw4 (anti-parallel diode of Sw4) starts conducting. A capacitive displacement current flows from the panel to the inductor in a resonance manner. So the inductor current is equivalent to the panel current. Voltage across the panel changes its polarity from positive to negative by means of the series-resonance. At the end of this resonance, voltage across the panel becomes -Vs/2.

Mode 2 (t2-t3): At the beginning of mode 2, Sw2

and Sw3 are turned on while Dsw2 (anti-parallel diode of Sw2) starts conducting. A case where the prior mode 1 guarantees a complete resonance, there is no current supplied from the input source at t=t2. The stored energy of the inductor is transferred to the lower voltage source (C2).

Mode 3 (t3-t4): Voltage across the panel maintains a critical -Vs/2 by means of the lower voltage source (C2). At t=t3, all inductor energy are transferred to the lower voltage source (C2). During this mode 3, the lower voltage source is applied to the inductor.

Mode 4 (t4-t5): At t=t4, Sw2 and Sw3 are turned off at the same time while Dsw3 (anti-parallel diode of Sw3) starts conducting. The capacitive displacement current of the panel flows via the inductor in a resonance manner. So the inductor current is equivalent to the panel current. Voltage across the panel changes its polarity from negative to positive due to the series-resonance. After finishing this resonance, voltage across the panel becomes Vs/2.

Mode 5 (t5-t6): At the beginning of mode 5, Sw1 and Sw4 are turned on while Dsw1(anti-parallel diode of Sw1) starts conducting. A case where the prior mode 4 guarantees a complete resonance, there is no current supplied from the input source (Vs) at t=t5. The stored energy of the inductor is transferred to the upper voltage source (C1).

Mode 6 (t6-t7): This mode returns to mode 1. At t=t6, the inductor current is zero.

Usually, PDP is operated from 80 to 200 (kHz) in practical applications. The operating frequency of the sustain driver depends on the characteristic of PDP in itself. The panel capacitance (CP) is determined by the panel size. In case of 42-inch diagonal panel, Cp is about 100 (nF) whereas a 7.5-inch panel has a small capacitive value approx. 2.5 (nF). However, the value of Cp is slightly varied with every change of on-off pixel states. In experiment, we use a 7.5-inch AC plasma display panel, and each sustain period is set to 1.5 (μs) under a fixed 200 (kHz) switching frequency. Each transition period of panel voltage is limited to 1 (μs). A case where series connected switches are located in a single arm, a sufficient dead-time should be properly preset to prohibit the switches from an arm short. In the proposed sustain driver, the dead-time is used as the period for the series-resonance.

III. Experimental Results

Fig. 3 shows experimental results of the proposed sustain driver. From Fig. 3(a) to Fig. 3(c), they show experimental results of voltage across the panel, current flowing through the panel, and input current before igniting. In these cases, PDP does not emit visible light; thus, only displacement current is flowing through the panel changing the polarity of the panel voltage. Two sub-voltage-sources are maintained a constant voltage level. From Fig. 3(d) to Fig. 3(f), they show experimental result during igniting with visible light. Discharging current flows through the panel. It is appeared at the end portion of panel current with following the displacement current. In this case, little current is supplied from the input voltage source (Vs). Voltage across the panel is slightly affected by means of the discharging current while the shape of the inductor current is constant.

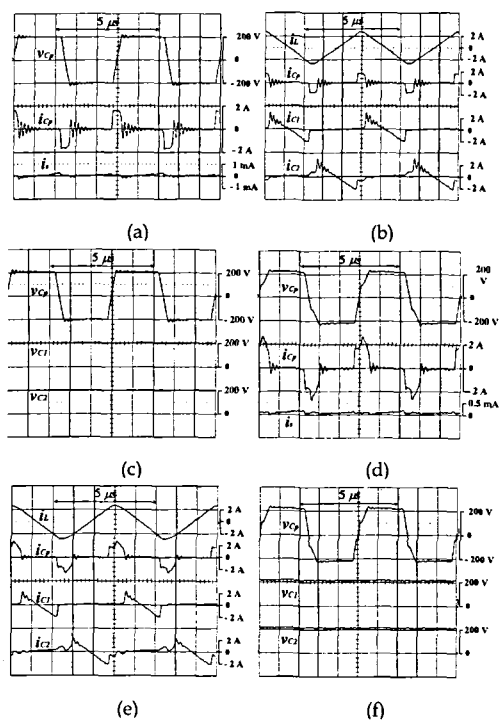

Fig. 3. Experimental results, (a) voltage across the panel, panel current, and input current before igniting, (b) inductor current, panel current, two external capacitor currents before igniting, (c) panel voltage, and two external capacitor voltages before igniting, (d) panel voltage, panel current, and input current after an ignition, (e) inductor current, panel current, two external capacitor currents after an ignition, (f) voltage across the panel, and two external capacitor voltages after an ignition.

For driving PDPs, it needs several voltage

sources having different voltage levels. Usually, additional dc-to-dc converters are required to generate the different voltage sources. In the viewpoint of power utility, it is desirable to select the main internal dc voltage level as that of sustain voltage because most power should be supplied for the sustain drivers. It hereby can minimize power conversion losses.

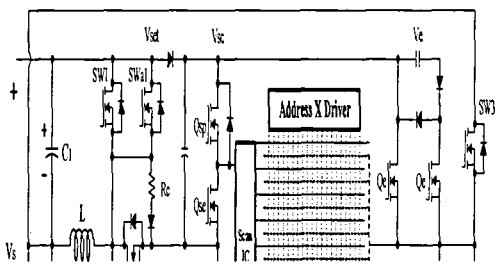

Fig. 4. Circuit configuration of the proposed sustain driver with embedded reset circuit

Fig. 4 shows a system set-up for the application of the proposed sustain driver with the reset circuit. Generally, the reset circuit needs a high voltage over 400 (V) to initialize the panel. In the proposed driver, the voltage source (Vs) can be directly used as a reset voltage. According to each period of ADS method, Qp controls the energy flow between the inductor (L) and the panel. During a sustain period, SW1 and Swa1 are operated in parallel. It can reduce the conduction loss dissipated by on-resistance of power MOSFETs. A case where it is operated in reset period, SW1 is turned off. SWa1 and SWa4 are conducting. The slop of the reset pulse depends on the time-constant; it multiplies RC by Cp.

IV. Conclusion

A new sustain driver and useful reset circuit composition scheme using a single voltage source were proposed for an efficient AC PDP drive. The proposed sustain driver uses a 2-level pulse and a series resonance between an external inductor and an intrinsic panel capacitance to recover the energy otherwise loss in charging and discharging of the panel. Although it requires a higher input voltage source, it has a compositional advantage because the input voltage source can be directly used as a reset voltage source.

Presentable achievements compared with the conventional similar approaches are 1) simple and efficient sustain driver, 2) low switching losses, 3) good energy recovery efficiency, and 4) useful reset circuit composition.

References

[1] A. Sobel, Plasma displays, IEEE Trans. Plasma Science, 19 (6) (1991) 1032-1047.

[2] J. W, The measurement, instrumentation, and sensors handbook, (CRC & IEEE Press, 1999).

[3] D. W. Parker, A. G. Knapp, T. S. Baller, The TV on the wall-has its time come? Proceeding of International Broadcasting Convention, (1997) 575-580.

[4] L. F. Weber, Measurement of wall charge and capacitance variation for a single cell in AC plasma display panel, Proceeding of Society for Information Display, 18 (1) (1977) 80-85.

[5] Y. K. Shin, C. H. Shon, W. Kim, J. K. Lee, The voltage-pulsing effects in AC plasma display panel, IEEE Trans. Plasma Science, 27 (5) (1999) 1366-1371.

[6] L. F. Weber, K. W. Warren, M. B. Wood, Power efficient sustain drivers and address drivers for plasma panel, U.S. Patent 4 866 349, Sept. 1989.

[7] H. B. Hsu, C. L. Chen, S. Y. Lin, K. M. Lee, Regenerative power electronics driver for plasma display panel in sustain-mode operation, IEEE Trans. Industrial Electronics, 47 (5) (2000) 1118-1125.

[8] C. U. Kim, F. S. Kang, J. H. Cho, W. S. Yoon, An efficient AC-PDP sustain driver employing boost-up function, Proceeding of IEEE IECON'02 Conf., Nov., 5-8, 2002, Seville, Spain, pp. 135-139.

[9] C. C. Liu, C. L. Chen, K. M. Lee, A novel energy-recovery sustaining driver for plasma display panel, IEEE Trans. on Industrial Electronics, 47 (6) (2000) 1271-1277.

[10] F. S. Kang, S. J. Park, C. U. Kim, A novel AC-PDP sustain driver based on dual resonance in sustaining mode operation, IEEE Trans. on Industrial Electronics, 50 (3) (2003) 536-545.