다단 변압기 기반 $3^{n-1}+2$ 레벨 PWM 인버터

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Cascaded-transformer-based $3^{n-1}+2$ level PWM Inverter

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요 약

본 논문은 $(3^{n-1}+2)$ 레벨 형성법에 기반한 멀티레벨 인버터를 제안한다. PWM 인버터, LEVEL 인버터와 다단 변압기로 구성되는 이 회로는 양질의 출력전압을 형성하기 위해서 이차측이 직렬로 결합된 다단 변압기를 이용하게 된다. 변압기 권선비의 적절한 선택을 통해 입력전압의 정수비 형태로 주어지는 출력전압레벨을 형성할 수 있다. 제안된 방식으로 11레벨, 29레벨 시작품을 제작하여 실험을 통해 타당성을 검증한다.

ABSTRACT

This paper presents a useful multilevel PWM inverter scheme based on a $(3^{n-1}+2)$ level generation technique. It consists of a PWM inverter, an assembly of LEVEL inverters, and cascaded transformers. To produce high quality output voltage waves, it synthesizes a large number of output voltage levels using cascaded transformers, which have a series-connected secondary. By a suitable selection of secondary turn-ratio of the transformer, the amplitude of an output voltage is appeared at the rate of an integer to an input dc source. Operational principles and analysis are illustrated in depth. The validity of the proposed system is verified through computer-aided simulations and experimental results using prototypes generating output voltages of an 11-level and a 29-level, respectively. And their results are compared with conventional counterparts.

키워드

harmonic distortion, multilevel systems, photovoltaic power systems, pulse width modulated inverters, transformer

Ⅰ. Introduction

Most of the power electronics technologies including control skills are required to convert the dc into ac power. A case where the amplitude of input voltage is low it needs an additional boost converter or a step-up transformer to obtain a high output voltage converting power from dc to ac, and commonly connected in series with a pulse width modulated inverter. However, somewhat high switching frequency of PWM inverter, and its dv/dt stress are resulted in low efficiency and occasionally electro magnetic interference (EMI) problem. In addition, an output filter is required to reduce high-switch-frequency components and to produce sinusoidal output from the inverter [1]-[6].

In points of alleviating these problems, multilevel inverters can substitute for the conventional PWM inverter. Multilevel topologies have been studied to increase the power reducing voltage stress on the power switching devices, and to produce high quality output voltages [7]-[15]. In the viewpoint of the latter, three presentable multilevel topologies can be considered, i.e., diode-clamped (or neutral-clamped) [12], flying capacitors (or capacitor-clamped) [13], and cascaded full-bridge cells with separate dc sources [14]. Theoretically, they can synthesize an infinite output voltage level. By increasing the number of output levels, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic

distortion. However, to increase output levels, they need a lot of switching devices, clamping diodes, or other passive elements. It, moreover, causes to the increase of complexity of switching patterns.

To mitigate these drawbacks, a novel multilevel PWM inverter employing cascaded transformers is presented in this paper. The most difference compared with the conventional multilevel schemes is that the proposed multilevel PWM inverter is separated into two inverter modules according to each functional purpose. One is a PWM inverter, and the other is an assembly of LEVEL inverters. The latter generates fundamental output voltage levels, and the former adds choppedpulses on each fundamental output level to obtain more sinusoidal output voltage waves.

Operational principle and analyses are illustrated in depth. To verify the validity of the proposed multilevel scheme, we carry out experiments with two kinds of inverter prototypes showing different output voltage shapes; one is an 11-level shaped PWM wave, and the other is a 29-level shaped PWM wave, respectively.

II. Proposed Multilevel PWM Inverter

Fig. 1 shows a compositional example of the proposed multilevel PWM inverter. It consists of three full-bridge inverters and their corresponding transformers, which have a series-connected secondary. Among full-bridge inverters, one is used for a PWM operation, and the other is an assembly of LEVEL inverters devoted to generate fundamental output voltage levels. In case of Fig. 1, it generates an 11-level shaped PWM output voltage wave.
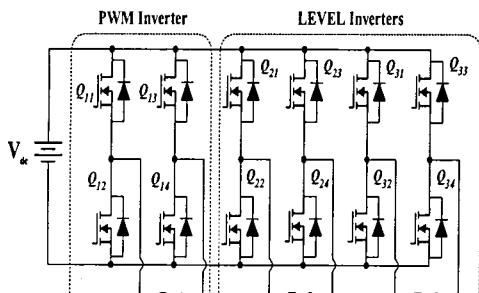

Fig. 1. Compositional example of the proposed multilevel PWM inverter to synthesize an 11-level shaped PWM output voltage.

By employing cascaded transformers, it increases the number of output voltage levels, whereas it decreases the numbers of switching

devices compared with conventional multilevel inverters. It also boosts low solar voltage to match that of ac utility. The leakage reactance of the cascaded transformers provides good filtering of the harmonics of the inverter voltage.
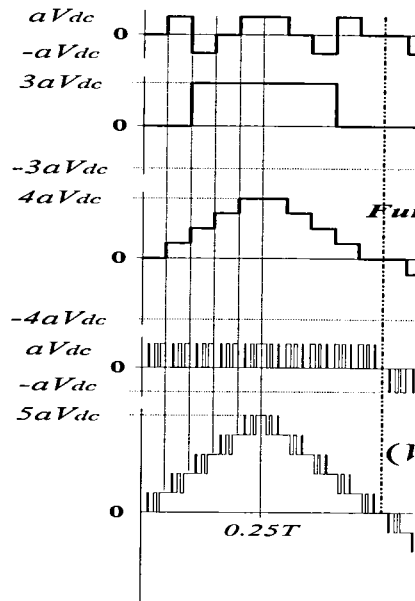

Fig. 2. Key waveforms in case of generating an 11-level shaped PWM output.

Fig. 2 shows key waveforms of the proposed multilevel PWM inverter depicted in Fig. 1. It includes a terminal voltage of PWM inverter (V1), output voltages of LEVEL inverters (V2, V3), and final output voltage (Vo). The number of a fundamental output voltage level is nine. It is synthesized by the sum of V2 and V3. Then V1 adds chopped pulses (a Vdc) on each fundamental level. As a result, the final output voltage (Vo) shows an 11-level PWM shaped wave.

Table I
Possible Output Level by Combination of Transformer

Cascaded Transformers	PWM	LEVEL			
	Tr. 1	Tr. 2	Tr. 3	Tr. 4	⋯
Turn-ratio	1:a	1:a	1:3a	1:9a	⋯

Table I lists possible output voltage levels by combination of cascaded transformers. The number of output level (N) is normalized by

$$N = 3^{n-1} + 2, \quad n = 1, 2, 3, \ldots \quad (1)$$

Here n means the number of selected transformers in sequence. The turn-ratio of Tr.1 is (1:a), and those of others are determined by 3n order. By applying proper switching functions to this configuration, the final output level can be generated by the rate of an integer to an input voltage source (Vdc). For example, if we select Tr.1, Tr.2, and Tr.3 as cascaded transformers, an 11-level can be obtained with PWM waveform. Fundamental nine output levels including zero (4aVdc, 3aVdc, 2aVdc, aVdc, and 0) is synthesized by the LEVEL inverters, and additional two levels (aVdc) are added from the PWM inverter.

III. Experimental Results

Fig. 3 shows experimental results of the 11-level PWM inverter equipped with three cascaded transformers. A switching frequency is set to 20 kHz, and a target output voltage and its frequency are 110 Vac and 60 Hz, respectively.
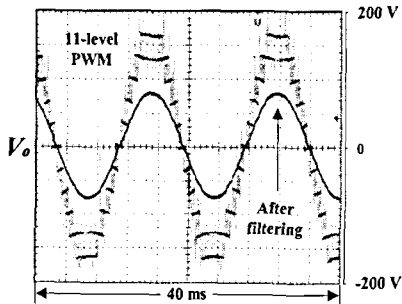

Fig. 3. Experimental result to 11-level

Although an output voltage of the 11-level PWM inverter shows nearly sinusoidal waves with the increase of load power, THD (total harmonic distortion) of the output voltage at no-load does not sufficiently satisfy the general requirement of 5 % below; therefore, we added a small capacitor to improve THD of output voltage at no-load and light load conditions. A value of the filter capacitor is 100 nF. Output voltage after filtering is superimposed on Fig. 3.

For the purpose of achieving more sinusoidal output voltage waves, we also tested a 29-level PWM inverter with four transformers, which have a series-connected secondary. Fig. 4 shows experimental results of terminal voltage of each transformer, and a final output voltage. The output voltage shows nearly sinusoidal waves, and dv/dt stresses imposed on switching devices are considerably reduced while it requires four full-bridge inverters and corresponding four transformers. In case of harmonic characteristics at a rated load condition, both inverters show almost same low THD (total harmonic distortion) as 1.332 % and 1.176 %, respectively. The 29-level PWM inverter shows better result in harmonic characteristics owing to the increased output levels.
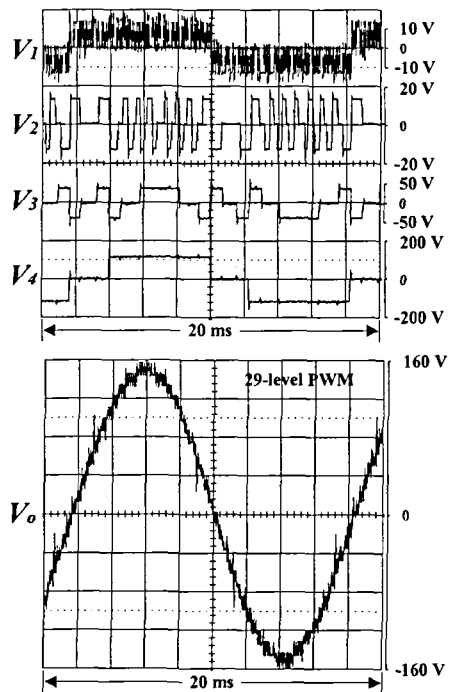

Fig. 4. Experimental result to 29-level

IV. Conclusion

Multilevel PWM inverter scheme was proposed in this paper. It can increase the number of output levels with considerably reduced number of switching devices compared with the conventional counterparts. Two kinds of multilevel PWM inverters synthesizing different output levels were tested by simulation and experiments.

Presentable achievements of the proposed multilevel scheme are summarized as (1) The generation of high quality output voltage waves by means of the increase of output voltage level, (2) Reduced number of switching devices compared with the conventional multilevel approaches, (3)

High-performance filtering effects due to the leakage reactance of cascaded transformers, (4) Low dv/dt stresses imposed on switching devices, (5) Less harmonic generation by the inverter in itself.

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