
Sensitivity Analysis of Plasma Charge-up Monitoring Sensor Using Neural Networks

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ABSTRACT

High aspect ratio via-hole etching process has emerged as one of the most crucial means to increase component density for ULSI devices. Because of charge accumulation in via hole, this sophisticated and important process still hold several problems, such as etching stop, loading effects during fabrication of integrated circuits. Indeed, the concern actually depends on accumulated charge. For monitoring accumulated charge during plasma etching process, charge-up monitoring sensor was fabricated and tested under some plasma conditions. This paper presents a neural network-based technique for analyzing and modeling several electrical performance of plasma charge-up monitoring sensor.

Keywords

SiO₂ etching, Plasma, Charge-up monitoring sensor, Neural networks

I. Introduction

Over the past few years, device size in modern semiconductor manufacturing has continuously decreasing as component density increases. And shifting towards the next generation ultra-large-scale integrated-circuits (ULSI), *SiO₂* via-holes etching with a high aspect ratio is a key process for fabrication of multilayer interconnects. Via etching for dual-damascene process with 0.18 μ m node or less requires high aspect ratio inter-metal dielectric (IMD) etching consisting of intermediate nitride and oxide layers or low-*k* dielectrics [1]. However, accumulated charge in high aspect ratio via holes during plasma etching have still unresolved difficulties; etching stop [2], micro-loading effect [3], and charge-up damage [4-6]. One of the most important problems is accumulated charge in via holes. Etching stop can be caused by a reduced transport of reactive species in deep and narrow structures, and the micro-loading effect by a local depletion of reactive species. Thus, it is expected that as the aspect ratio of via holes increase, the much more accumulated charge is significant in ULSI.

In *SiO₂* etching process using fluorocarbon gas plasmas, a fluorocarbon film is deposited on the underlayer surface and sidewall of the via holes. In fact, the deposited fluorocarbon

polymer have influence upon the etching characteristics and charge accumulation in *SiO₂* via holes etching process [7]. To accomplish an optimal high aspect ratio etching process for next generation device fabrication, it will be very significant work to monitor and control the amount of charge accumulated in *SiO₂* layer.

In Section II, charge-up monitoring sensor to finally measure charge accumulated in high aspect ratio via holes and measurement are introduced. To make firm the functionality of the sensor, charging potential between two electrodes is measured during *Ar* plasma discharge. The general concept of neural networks (NNs) is provided in Section III, followed by an analysis of experiment with NNs and response surface plots. Finally, in Section IV, results and discussion are presented, followed by conclusion in Section V.

II. Experiment and measurement

According to experienced bowing of high aspect ratio via hole etching in *SiO₂* dielectrics, a major reason for the via-hole bowing was converged to the charge accumulation on the sidewall due to fluorocarbon polymer. When *SiO₂* film is etched under fluorinated plasma, such as *C₄F₈* or *C₂F₄*, it generates many high molecular weight radicals (*C_xF_y* radicals) that

contribute to the fluorocarbon polymer deposition. Recently, it has been reported that the deposited fluorocarbon on sidewall of via-hole patterns is conductive, and this can cause mitigation of accumulated electric charge [8].

An intention of developing the charge-up damage sensor is to monitor SiO_2 etching process in real-time as regards accumulated charge. On a 2" $Si <100>$ wafer, 300nm of silicon dioxide layer was thermally deposited. On the top electrode, a great number of 300nm vias in their diameters were formed to perform high aspect ratio (=1:5) via hole etching process. For more high aspect ratio, either/both thinner IMD SiO_2 and/or smaller via size was desired, but this was the critical fabrication capability under the university research environment. However, 1:5 aspect ratio was high enough to performing sidewall conductivity measurement. Figure 1 shows a schematic of the structure of fabricated charge-up sensor.

To verify the performance of the fabricated damage sensor, the charging potential of two polycrystalline silicon electrodes was measured after via-etching is completed.

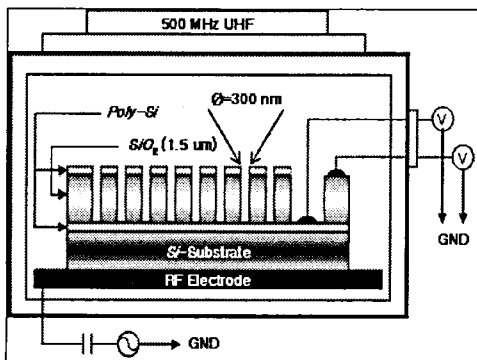


Figure 1. A schematic of charge-up damage sensor

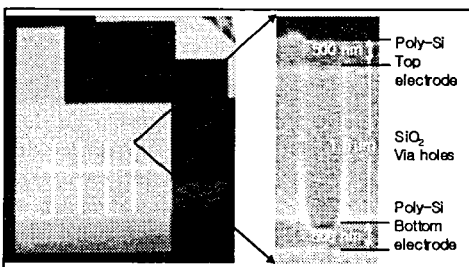


Figure 2. A cross sectional SEM photo of fabricated sensor with 300nm via holes

A cross sectional SEM photograph is presented in Figure 2. In this exercise, a home-made UHF (500MHz) plasma reactor was employed. This etching system provides the mean electron energy was about 2-3eV, and the electron density was about $10^{11} cm^{-3}$.

The charge-up sensor was located on the RF electrode in the plasma reactor (see Figure 1). While Ar plasma was irradiated, DC potential between the top and the bottom electrodes was measured.

(b) III. Sensitivity analysis

An NN is a structured interconnection of computational nodes called "neurons" that contribute to parallel computation in a manner similar to the human brain. Each neuron contains the weighted sum of its inputs filtered by a neuron activation function, providing NNs with the ability to generalize with an added degree of freedom that is not available in traditional regression techniques [9]. Due to their inherent ability to learn complex nonlinear mappings, NNs have been successfully applied to semiconductor process modeling, optimization, and control [10]. Three input factors with three levels of each were considered: pressure, source power, and bias power. The response of interest was the potential difference measured (refer to Table 1).

Utilizing Obornns (Object Oriented Neural Network Simulator), which is a custom NN simulation package developed by the Intelligent Semiconductor Manufacturing Group at Georgia Tech, were derived. After setting up percentage used for training and test, NN were trained with the data generated from the 3^3 factorial designed experiments. Among the input and output of the networks, there are hidden neurons which extract nonlinear features from the data, and several networks with different numbers of hidden neurons were performed until RMS error is below target. Model performance is depicted graphically in Figure 3.

IV. Result and discussion

Under higher pressure with Ar plasma irradiation, dissociated reactive ions are tend to

Input factor			
Name	Abbrev.	Range	Unit
Pressure	PRES	5, 15, 25	<i>mTorr</i>
Bias Power	Bias_PWR	1, 25, 50	watts
Source Power	Src_PWR	500, 750, 1000	watts
Response			
Name	Abbrev.	Unit	
Potential Difference	V_Dif	V	

Table 1. Process parameters, unit, and ranges

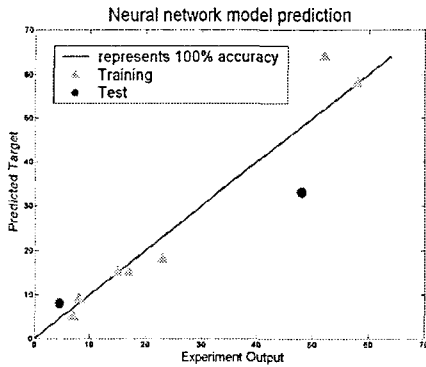


Figure 3. Performance evaluation of process

more like to get directed vertically rather than a condition of lower pressure plasma. Thus, charging potential under higher pressure can be less than others.

Once the neural process model was established, response surfaces were generated to explain on the relationships between any two process parameters of three and an interesting response. On the other hand, the remaining factor was set to at its mid-range level.

Figure 4(a) presents the effect of Bias and source power on the degree of the potential difference when the pressure is hold to 15 *mTorr*. At a given bias and source power, the accumulated charge slightly increases. The graph presents very low curvature near the middle range of source power. This means low degree of correlation between process parameters and the response. However, as bias power increases and source power is in the middle of the range, the accumulation charge distribution is somewhat notable. An observed pattern in Figure 4(b) is similar to Figure 4(a).

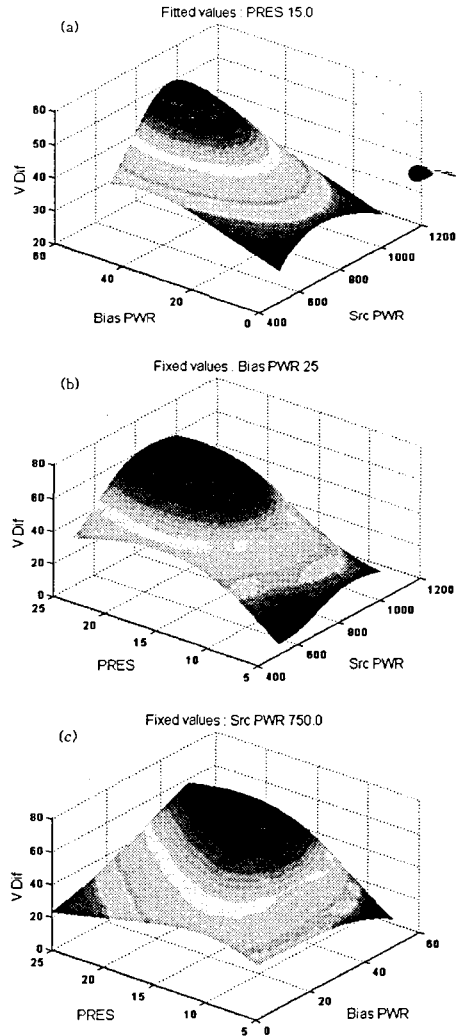


Figure 4. Response surface plots for V_Dif

There are little point in Figure 4(c). But, high bias power and pressure is worthy of notice about the aspect of accumulated charge. This need to be further investigation.

V. Conclusion

To summarize, a sensor fabrication and a measurement of charging potential under *Ar* plasma discharge as a method of accumulated charge in via hole patterns. An useful method for measuring accumulated charge using the fabricated charge-up damage sensor has generated. And the response surface method

was also shown to identify suitable process conditions to avoid plasma charge damage, which is one of the most crucial problems.

Reference

- [1] Ogawa E.T, Lee K.D, Matsuhashi H, Ko K.S, Justison P.R, Ramamurthi A.N, Bierweg A.J, Ho P.S, Blaschke V.A, Havemann R.H, "Statistics of electromigration early failures in Cu/oxide dual-damascene interconnects", *Reliability Physics Symposium, 2001. Proceedings. 39th Annual. 2001 IEEE International*, pp. 341-349, 30 April-3 May 2001
- [2] S. Samukawa and T. Mukai, "High-performance of process-induced charging in scaled-down devices and reliability improvement using time-modulated plasma", *J. Vac. Sci. Tech. B*, vol. 18, no. 1, pp.166-171, 2000
- [3] C. Hedlund and S. Berg, "Microloading effect in reactive ion etching", *J. Vac. Sci. Tech. A*, vol. 12, no. 42, pp. 1962-1965, 1994
- [4] T. Nozawa and T. Kinoshita, "The electron charging effects of plasma on notch profile defects", *Jpn. J. Appl. Phys., Part I*, vol. 34, no. 4B, pp. 2107-2113, 1995
- [5] T. Kinoshita, M. Hane, and J. P. McVittie, "Notching as an example of charging in uniform high density plasmas", *J. Vac. Sci. Tech. B*, vol. 14, no. 1, pp. 560, 1996
- [6] K. Hashimoto, "New phenomena of charge damage in plasma etching: heavy damage only through dense-line antenna", *Jpn. J. Appl. Phys., Part I*, vol. 32, no. 12B, pp. 6109-6113, 1993
- [7] T. Simmura, S. Soda, S. Samukawa, M. Koyanagi, and K. Hane, "electrical conductivity of sidewall deposited fluorocarbon polymer in SiO₂ etching processes", *J. Vac. Sci. Tech. B*, vol. 20, no. 6, pp. 2346-2350, 2002
- [8] T. Simmura, S. Soda, S. Samukawa, K. Hane, "Mitigation of Accumulated Electric Charge by Deposited Fluorocarbon Film during SiO₂ Etching", *J. Vac. Sci. Tech. A*, vol. 22, no. 2 pp. 433-436, Mar/Apr 2004
- [9] C. Himmel and G. Mary, "Advantages of plasma etch modeling using neural networks over statistical techniques", *IEEE Trans. Semiconductor Manufacturing*, vol. 6, no. 2, pp. 103-111, May 1993
- [10] G. May, "Computational intelligence in micro-electronics manufacturing", in *The Handbook of Computational Intelligence in Design and Manufacturing*, J. Wang and A. Kusiak, Eds. Boca Raton, FL: CRC press, 2001, Ch. 13