Dislocation-Free Shallow Trench Isolation 공정 연구

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A study on the Dislocation-Free Shallow Trench Isolation (STI) Process

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Abstract : Dislocations are often found at Shallow Trench Isolation (STI) process after repeated thermal cycles. The residual stress after STI process often leads defect like dislocation by post STI thermo-mechanical stress. Thermo-mechanical stress induced by STI process is difficult to remove perfectly by plastic deformation at previous thermal cycles. Embedded flash memory process is very weak in terms of post STI thermo-mechanical stress, because it requires more oxidation steps than other devices. Therefore, dislocation-free flash process should be optimized.

Key Words : Shallow Trench Isolation (STI), Dislocation, Gate Oxide, Thermo-Mechanical Stress, Wet/Dry Oxide

1. Introduction

Shallow trench isolation (STI) is the most favorable scheme for advanced integrated circuits. While STI process give benefits due to its scalable characteristics, it is known to raise problem like STI induced dislocation.[1~2] One of the most critical issues is to reduce stress related defects as resulted from STI profile, liner material, gap-fill material, and annealing, etc. They play an important role in dislocation generation. Therefore, STI related those processes is dependent on device characteristics. Recently, many groups have been studied root cause of STI stress and its solution to reduce dislocation. In general, shallower trench depth, taper trench angle[3], and pull back process[1] are reported to be helpful to reduce device failure by dislocation. Especially, trench top corner rounding is believed to be necessary not only to relax stress but also to improve device characteristics. In several experiments, we find out the development of defects according to the variation of the heat cycle in the STI integrity. And the stress induced by the intrinsic force and the residual mechanical force which remains not relaxed by inelastic deformation at the previous heat cycle. Therefore, every processing should be optimized in STI integration. In addition, another critical issue of STI process is to reduce the stress generation during oxidation steps such as the gate oxidation. In a view thermal stress, dry oxidation gives more stress due to its long time and high temperature. Therefore, wet oxidation was used to gate oxide due to its beneficial properties. But we obtained dislocation free wafer by changing gate oxide from wet to dry in this work. In this point of view, flash memory technology is considered to be more difficult to integrate process than other devices, because it requires more thermal budget and oxidation. In this work, various experimental results and their mechanisms will be provided, and the relationship between stress by STI and gate oxidation ambient will be mainly discussed. And we compared wet oxidation with dry oxidation for gate oxide.

2. Experiment

The device used for this study is fabricated with 0.18 μm embedded flash technology on (100) silicon wafers. The generated defects have been observed through SEM view after wright decoration. All thermal processes from STI CMP to BPSG Annealing are processed with N_2 ambient. In this process, STI densification temperature (Post CMP annealing; N_2, 900 °C) is relatively higher than others. Wet oxide and dry oxide were used to gate oxide. Additionally, 750 °C and 800 °C wet oxidation, and 800 °C and 850 °C dry oxidation are tried respectively to know dependency on oxidation growth rate. Oxidation conditions are 10.5 nm, 800 °C, H_2, HCl, O_2 for screen oxidation, 9.6 nm, 750 °C, H_2, HCl, O_2 for tunnel oxidation, 13.0 nm, 800 °C, H_2, HCl, O_2 for Gate oxide-1.

3. Result and Discussion

In the early development stage, a large portion of pin leakage failure was found in embedded flash product. As a result of transmission electron microscope (TEM) analysis, the root cause is proven to be a dislocation as shown in Fig. 1.

Simple process flow of embedded flash memory is shown in Fig. 2, which processes related to thermo-mechanical stress are mainly described. Comparing with logic process, flash technology needs additional processes like tunnel oxide, floating gate poly, oxide-nitride-oxide (ONO) , and flash high voltage (~ 10 V) gate oxide. To find critical process with related to dislocation, defects have been inspected at process colored with closed box in Fig.2. As a result, gate oxide-1 is revealed to be major factor to generate defect shown in Fig.3 (a)

Fig. 1. Cross-sectional TEM image of dislocation induced by stress.(white arrow)

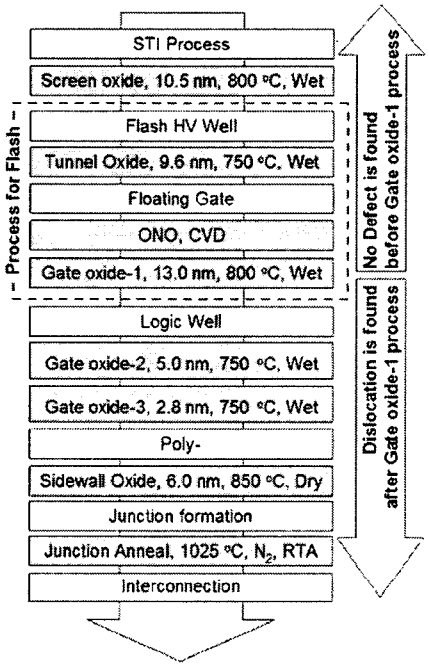

Fig. 2. Simple process flow of embedded flash, processes related to stress are mainly described.

In order to verify the effect of oxidation ambient and oxide growth rate, dry oxidation instead of wet oxidation is tried for gate oxide-1 in Fig.2. After treatment of dry oxidation, any dislocation pit is not found as shown in Fig.3(b). Irrespective of temperature/oxidation rate, defect density is only dependent on oxidation ambient. Interestingly, wet oxidations at the previous step like screen oxidation and tunnel oxidation as shown in Fig.2, don't give any hurt to wafer. Although nearly same recipe is applied, only gate oxide-1 causes dislocation pit. That means that hydrogen atom apparently enhances the occurrence of dislocation, but its behavior is believed to depend on wafer status.

In order to clarify root causes of dislocation, we performed some experiments as shown in table 1.

After wet-etching gate oxide-1 in the local region, another 5.0 nm gate oxide, so called gate oxide-2, have been grown by wet and dry oxidation. In the region covered by both dry oxidation conditions, any defects are not found. But in the denuded region, not dry oxidation but wet oxidation ruptures wafers as described in table 1.

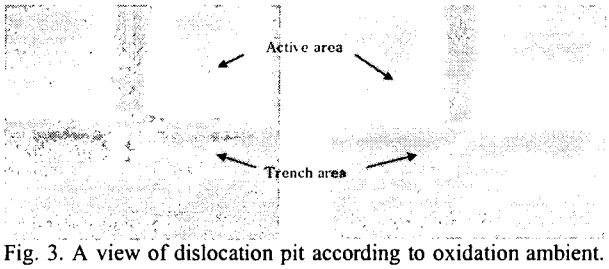

Fig. 3. A view of dislocation pit according to oxidation ambient. Oxide thickness is 13.0 nm. (a) Wet oxidation with H_2, HCl and O_2 ambient, (b) Dry Oxidation with only O_2.

Gate Oxide-1/ Gate Oxide-2	Dislocation		
	Cell region	Flash HV Region	LV Region
Wet Oxide/Wet Oxide	No	Many	Many
Dry Oxide/Wet Oxide	No	No	Many
Dry Oxide/Dry Oxide	No	No	No

Table 1. The result of defect monitoring for each region.

4. Conclusion

Intrinsic and residual mechanical stresses induced by STI process are accumulated by subsequent process, and finally wet oxidation makes it rupture. Especially, when STI top corner is opened by the repetition of oxidation and removal, and it is oxidized with hydrogen ambient, severe dislocation pit was found. In manufacturing embedded flash, dislocation free wafer is obtained by changing gate oxide from wet to dry. Consequently, we considered that using a dry oxidation is a suitable method for dislocation free wafer in embedded flash.

Acknowledgement

This work was supported by Grant No. R01-2002-000-00375-0 from the Basic Research Program of the Korea Science & Engineering Foundation.

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