Electrical Characteristics of Ge-Nanocrystals-Embeded MOS Structure

Samjong Choi[1,2], Byoungjun Park[1], Hyunsuk Kim[1], Kyoungah Cho[1] and Sangsig Kim[1,*]

[1]*Department of Electrical Engineering and Institute for Nano Science, Korea University, Seoul 136-701, Korea*

[2]*Manufacturing Technology Team 1, Memory Division, Semiconductor Business, Samsung Electronics Co., Gyeonggi-Do 445-701, Korea*

Abstract : Germanium nanocrystals(NCs) were formed in the silicon dioxide(SiO_2) on Si layers by Ge implantation and rapid thermal annealing process. The density and mean size of Ge-NCs heated at 800 ℃ during 10 min were confirmed by High Resolution Transmission Electron Microscopy. Capacitance versus voltage(C-V) measurements of MOS capacitors with single Al_2O_3 capping layers were performed in order to study electrical properties. The C-V results exhibit large threshold voltage shift originated by charging effect in Ge-NCs, revealing the possibility that the structure is applicable to Nano Floating Gate Memory(NFGM) devices.

Key Words : Ge, nanocrystals, Al_2O_3, ion implantation, memory

1. INTRODUCTION

Nano-floating gate memory (NFGM) based on metal-oxide-semiconductor (MOS) structures has recently attracted interest due to the potential application in next-generation integrated flash memory. In NFGM, nanocrystals (NCs) are embedded as charge-storage nodes in an oxide layer between the control gate and the tunneling layer to replace the continuous floating gate layers in conventional flash memories [1]. The use of NCs in NFGM offers smaller operating voltages, better endurance characteristics, and faster write/erase speeds than conventional flash memories [2]. Si NCs have widely been utilized for the fabrication of NFGM [3]. However, Ge NCs have more recently been researched due to their smaller band gap than Si NCs [4]. The smaller band gap provides the higher confinement barrier for the retention mode and the smaller barrier for the program and erase modes.

A variety of deposition methods for Ge NCs including sputter deposition, rapid thermal annealing (RTA) of chemical-vapor-deposition, and pulsed-laser deposition have been employed for the fabrication of NFGM. Recently, Ge NCs synthesized by RTA of implanted Ge ions in SiO_2 have been researched for the simpler fabrication of NFGM than that prepared by the depositions [4].

In this paper, we investigate electrical characteristics of Ge-NCs-Embeded MOS structure.

2. EXPERIMENT

50-nm-thick SiO_2 films were grown by thermal oxidation of (100) *p*-type Si substrates, and the films were implanted at room temperature with $^{74}Ge^+$ions at 30 keV with a dose of $2x10^{16}$ /cm^2 for the fabrication of NFGM based on MOS capacitors. The dose of ions and the kinetic energy of ions were determined using a TRIM(transport of ions in matter) simulation code. Single capping Al_2O_3 layers were deposited on the SiO_2 films at a growth temperature of 300℃ with Atomic Layer Deposition technique. Trimethylaluminum (TMA) and distilled water were utilized as the precursors for the Al_2O_3 deposition. The Ge-implanted films deposited with the single capping Al_2O_3 layers were annealed in N_2 gas ambient for 10 min at 800 ℃ before aluminium deposition of gate electrodes.

The high-frequency (1MHz) C-V was measured by a HP 4285A *LCR meter*. A *high-resolution transmission electron* microscope (HRTEM, Tecnai F30) was used to obtain the cross-sectional and planar HRTEM images of the capacitors. All measurements were carried out at room temperature.

3. RESULTS AND DISCUSSION

Cross-sectional HRTEM image was taken for the Ge-NCs-embeded MOS capacitor with a single capping Al_2O_3 layer of a 13-nm thickness. The distribution of the Ge NCs in the 30-nm range is largely consistent with the calculated concentration profile of Ge ions in the as-implanted film by a TRIM code (Fig. 1). Although the wing of the profile reaches significantly the interface, the control and tunneling oxide layers are defined clearly in the HRTEM image any Ge NCs may not be seen in the 8-nm thick region of SiO_2 near the Si/SiO_2 interface. Each of the NCs has a single-crystal phase, and the average size of the NCs is about 4 nm. The NCs embedded in the SiO_2 are isolated from each others. The average concentration of the NCs estimated from the HRTEM image is $4x10^{17}$ /cm^3 in a unit volume and $2x10^{12}$/cm^2 on a vertical unit area: the average

concentration on a planar unit area near the interface should be smaller than that on a vertical unit area.

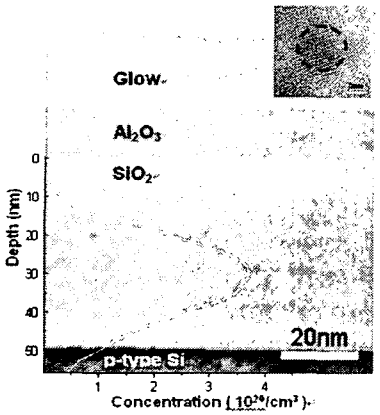

Fig.1. Cross sectional HRTEM image

High-frequency C-V characteristics of the Ge-NCs-embeded MOS capacitor with the Al_2O_3 layer are investigated as the gate voltage sweep range is gradually increased. Flatband voltages(Vfb) of each samples have been presented in Fig. 2. The concentrations of hole and electrons for the applied voltages of ±20 V are largely closed to the average concentrations of the Ge NCs estimated from the HRTEM image indicating that only the Ge NCs near the interface are charged for these voltages through tunneling oxide.

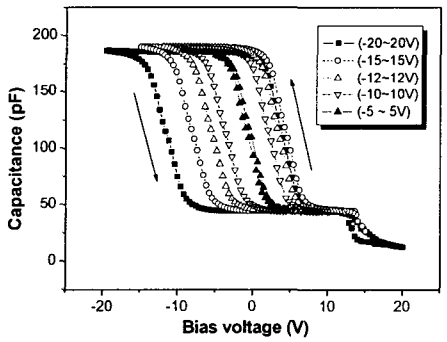

Fig 2. C-V curves of Ge-embeded MOS capacitor

For the Ge-NCs-embeded MOS capacitors with the Al_2O_3 layer, the C-V curves obtained in the forward and reverse C-V sweep in a range from -20 to 20 V in the dark and under the illumination of the white light are compared in Fig. 3. Under the illumination, the lower capacitance part in the sweep from -10 to 20 V is enhanced, and the dropping of the capacitance in the range of 10 to 20 V observed in the dark is absent: this drop is due to the deep depletion [3]. These findings originate from the narrowing of the depletion layer in the p-type Si substrate caused by the photogeneration of holes. The photogeneration of holes by the light increases the concentration of main carriers in the region where the electrical field induced by the gate voltage reaches.

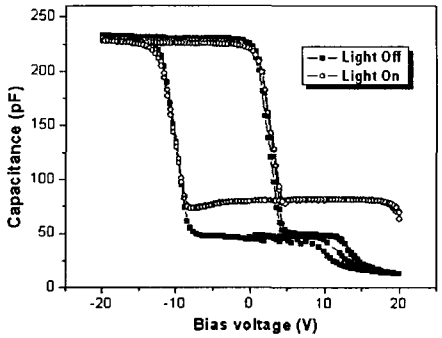

Fig.3. C-V curves in the dark and under the illumination of white light.

4. CONCLUSION

Ge NCs were formed by ion implantation and thermal annealing at 800 ℃ under a high-purity N_2 atmosphere. The density and diameter of Ge NCs were $2x10^{12}$ /cm^2 and 4 nm, respectively. The C-V results exhibit large threshold voltage shift originated by charging effect in Ge-NCs, revealing the possibility that this structure is applicable to Nano Floating Gate Memory(NFGM) devices. In addition, the illumination of white light enhances the lower capacitance part of the C-V hysteresis by the reduction of the depletion layer due to the photogeneration of holes.

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