2005년도 대한전기학회 전문대학교육위원회 학술대회 논문집 2005.10.14-10.15

제어기 성능을 고려한 전압형 인버터의 출력 LC필터 설계

민완기, 김재식*, 최재호**
조선이공대학 전기과, *포스콘기술연구소, **충북대학교 전기전자공학부

Output LC Filter Design of Voltage Source Inverter Considering the Performance of Controller

Min Wan Ki, Kim Jae Sig*, Choi Jae Ho**
Chosun College of Science & Thechnology, *POSCON R&D Center, **Chungbuk National University

Abstract - The LC filter design procedure of the inverter output filter is described. The transfer function of the filter output voltage to the load current is described with the capacitor value and the system time constant considering the system controller. By using the closed form of the relation between the filter capacitor value and the system time constant, the capacitor value can be calculated with the given system time constant and vice versa. It is more practical for the implementation of power and control circuit of inverter. And as the effect of the load current to the voltage distortion can be calculated from the closed form, it is possible to analyze the system how much the voltage waveform is distorted in case of the nonlinear load. All the proposed design procedure is verified with the simulation and experimental results.

I. INTRODUCTION

The AC power supply such as UPS(Uninterruptible power supply) inverter requires a L-C low-pass filter at the output side to reduce the harmonics generated by the pulsating modulation of voltage waveform. For the design of L-C low-pass filter, the cut-off frequency of filter is considered to be able to eliminate the most low order harmonics of the output voltage waveform. To operate as an ideal voltage source, that means no additional voltage distortion even though under the load variation or a nonlinear load, the output impedance of the inverter must be kept zero. Therefore, the capacitance value should be maximized and the inductance value should be minimizedat the selected cut-off frequency of the low-pass filter. But, as increasing the capacitor value, the inverter power rating will be increased due to the increase of the reactive power of the filter. The capacitor value should be limited to some value and the inductance value should be increased as much as the decrease of capacitor value. So it is basically difficult to get the zero output impedance so far as the L-C filter is used.[1] Theoretically, the output impedance of a PWM inverter can be controlled by the gain and bandwidth of its voltage regulating loop.[2] But the system control response is limited as the structure of the controller, inverter switching frequency, and the sampling speed of the microprocessor. Therefore, in the conventional filter design procedure, the component values of L-C filter are usually modified when we establish the feedback controller of an inverter.

A lot of studies have been accomplished on the optimal L-C filter design. Most of them are based on the cost function defined by the reactive power rating of the filter components under the steady state condition.[3,4] Each value of L and C component is determined to minimize the reactive power in these components. But, if the value of L-C filter is selected to minimize the cost function, then it is common that the filter components are determined at the set of a small capacitance and a large inductancein the previous studies, and consequently the output impedance of the inverter is so high. With these design values, the voltage waveform of the inverter output can be sinusoidal under the linear load or steady state condition. But in case of a step change of the load or a nonlinear load, the output voltage waveform will be distorted cause by the slow system response.

The distortion of voltage waveform can be mitigated with an additional voltage feedback controller. But its performance is limited as the time constant of the controller, inverter switching frequency, and the sampling speed of microprocessor. Therefore, the filter design values should be modified through the try and error method as the performance of the controller to reduce the distortion of the voltage waveform as mentioned above. So if the relation between the distortion of the voltage waveform and the performance of the controller can be described as the closed form, then it may be possible to design the L-C filter of inverter considering the performance of the system controller.[5]

This paper describes the design procedure of the inverter output filter. The transfer function of the filter output voltage to the load current is described with the capacitor value and the system time constant considering the performance of the system controller. This means thatthe relation between the filter capacitor value and the system time constant is given as the closed form. By using the closed form of the relation between the filter capacitor value and the system time constant, the capacitor value can be calculated with the given system time constant and vice versa. It is more practical for the implementation of power and control circuit of inverter. And as the effect of the load current to the voltage distortion can be calculated from the closed form, it is possible to analyze the system how much the voltage waveform is distorted in case of the nonlinear load.

The proposed design procedure of VSI output filter is well organized schematically with a flow chart and verified with the simulation and experimental results.

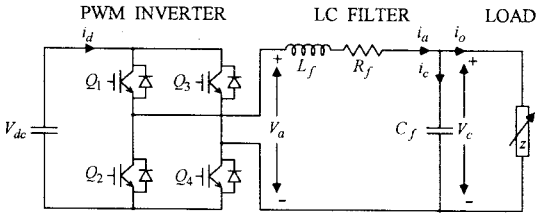


Fig. 1. Power circuit of single phase PWM-VSI.

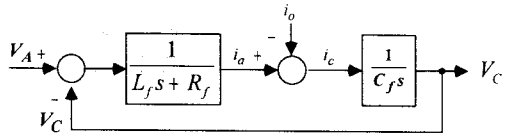


Fig. 2. Block diagram of single phase PWM-VSI.

II. SINGLE-PHASE PWM-VSI SYSTEM

Figure 1 shows the power circuitof the single phase PWM-VSI with any linear or nonlinear load. The load current flows differently depending on the various kinds of loads such as linear and nonlinear load. Therefore it is difficult to represent the transfer function of inverter output voltage to load current. But the plant composed of L-C low-pass filter satisfies linear property, so it is possible to represent MISO(Multi Input Single Output) system which has two inputs of inverter output voltage and load current. Figure 2 shows the system block diagram of the single phase PWM-VSI and the input and output transfer function is expressed as (1).

$$V_C(s) = \frac{1}{L_f C_f s^2 + R_f C_f s + 1} V_A(s) - \frac{L_f s + R_f}{L_f C_f s^2 + R_f C_f s + 1} I_O(s) \quad (1)$$

The frequency transfer function for the harmonics analysis of the output voltage waveform according to two inputs is described as (2).

$$V_C(j\omega) = \frac{1}{1 - L_f C_f \omega^2 + j R_f C_f \omega} V_A(j\omega) - \frac{j L_f \omega + R_f}{1 - L_f C_f \omega^2 + j R_f C_f \omega} I_O(j\omega) \quad (2)$$

Form (2), the amplitude of the voltage harmonics of the filter output can be calculated by summing the two harmonics caused by the inverter output voltage and by the load current. Equation (2) can be simplified as (3) by neglecting the imaginary term of the denominator, because the ESR of the inductor is very small and it means that $|1 - L_f C_f \omega^2| >> |R_f C_f \omega|$.

$$V_C(j\omega) = \frac{1}{1 - L_f C_f \omega^2} V_A(j\omega) - j \frac{L_f \omega}{1 - L_f C_f \omega^2} I_O(j\omega) \quad (3)$$

In the conventional output filter design method, the load current is treated as the disturbance and so the second imaginary term of (3) is neglected.[3,4]The cut-off frequency of the L-C filter is calculated first, and then the optimal value of the each filter component is selected which minimizes the cost function defined by the sum of the reactive power. This filter design procedure can be well applied to the linear load. But in case of nonlinear load or transient load change, the imaginary term of (3) can not be neglected due to the increase of load current harmonics. Therefore, for the analysis of voltage harmonics under the nonlinear load, the imaginary term of (3) should be considered.
In (3), to be independent on the load current, the inductor value should be minimized and on the contrary maximized the capacitor value at the same cut-off frequency. Then it satisfies the zero output impedance and works as an ideal voltage source. But as mentioned before, the inverter power rating will be increase as the increase of capacitor value. So the capacitor value can be limited with the help of fast feedback voltage controller. It is clear that the filter design value should be compromised as the performance of the system controller.

III. RELATION BETWEEN CONTROLLER RESPONSE AND HARMONICS

The CDM(Coefficient Diagram Method) controller with observer canonical form is used in the filter design.[6] The system block diagram including CDM controller is shown in Fig. 3, and the transfer function can be represented as (4).

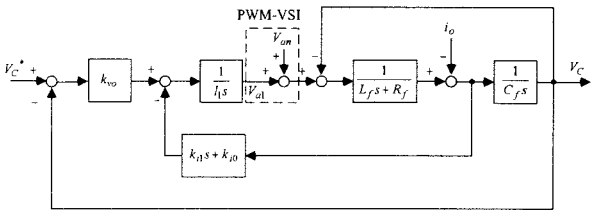


Fig. 3. System block diagram with controller.

$$V_C(s) = \frac{k_{v0}}{L_f C_f l_1 s^3 + (R_f l_1 + k_{i1}) C_f s^2 + (l_1 + k_{i0} C_f) s + k_{v0}} V_C^*(s) - \frac{l_1 L_f s^2 + l_1 R_f s}{L_f C_f l_1 s^3 + (R_f l_1 + k_{i1}) C_f s^2 + (l_1 + k_{i0} C_f) s + k_{v0}} I_o(s) \quad (4)$$

Using the stability index 1=2.5, 2=2 proposed by Manabe in Ref. [6] and selecting the coefficients of the characteristic equation as Eq. (5), CDM controller can be designed as robust controller which doesn't overshoot.

$$M(s) = \frac{1}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} = \frac{1}{\frac{a_0 \tau^3}{\gamma_2 \gamma_1^2} s^3 + \frac{a_0 \tau^2}{\gamma_1} s^2 + a_0 \varpi + a_0} \quad (5)$$

In CDM controller defined by (5), the time constant()for unit step response is defined by a_1/a_0 and the settling time is to be 2~2.5. The first term of (4) has the characteristic of low-pass filter and the gain in the pass band range of the system transfer function is uniformly maintained of 0[dB], so the characteristicequation in the range becomes to be fixed for k_{v0}like the numerator. Therefore, for the load current harmonics which exist within the band pass range, the transfer function of the filter output voltage harmonics to the load current harmonics can be described simply by neglecting the term of the ESR of inductor.

$$\frac{V_C(j\omega)}{I_O(j\omega)} = \frac{n^2 l_1 L_f \omega_0^2}{k_{v0}} \quad (6)$$

where

$\omega_0 = 2\pi f$: fundamental angular frequency

By comparing the coefficients of (4) and (5), kv0can be determined. The transfer function of the output voltage to the load current is driven after substitution in (6) from the relation between the time constant() of the controller and the value of the filter capacitance as (7)

$$\frac{V_C(j\omega)}{I_O(j\omega)} = \frac{n^2 \omega_0^2 \tau^3}{12.5 C_f} \quad (7)$$

From (7), under the given specification of voltage harmonics, the capacitor value can be determined to the time constant() of the controller and vice versa. The inductor value is obtained by the relations between the selected capacitance and the cut-off frequency.

IV. NECESSARY PROCEDURE IN FILTER DESIGN

The filter design is performed as follows:

1) Establishment of the necessary hypothesis of the filter specification and progress.
2) Analysis of the filter and establishment of the design method.
3) Theoretical development according to the established method.
4) Presentation about the example of the filter design and comparison with the simulation.

A. Filter specification and hypothesis

The filter design specification and hypothesis are performed as follows:

Specification

1) Linear load is 1~0.8 lagging load.
2) Nonlinear load is a rectif ier load with CF=3.
3) THD is below 5% in case of both linear and nonlinear load.
4) MI(Modulation Index) is 0.8 in the rated resistor load

Assumption

1) The plant with LC filter is linear.
2) The current is an ideal sinusoidal wave in case of the linear load.

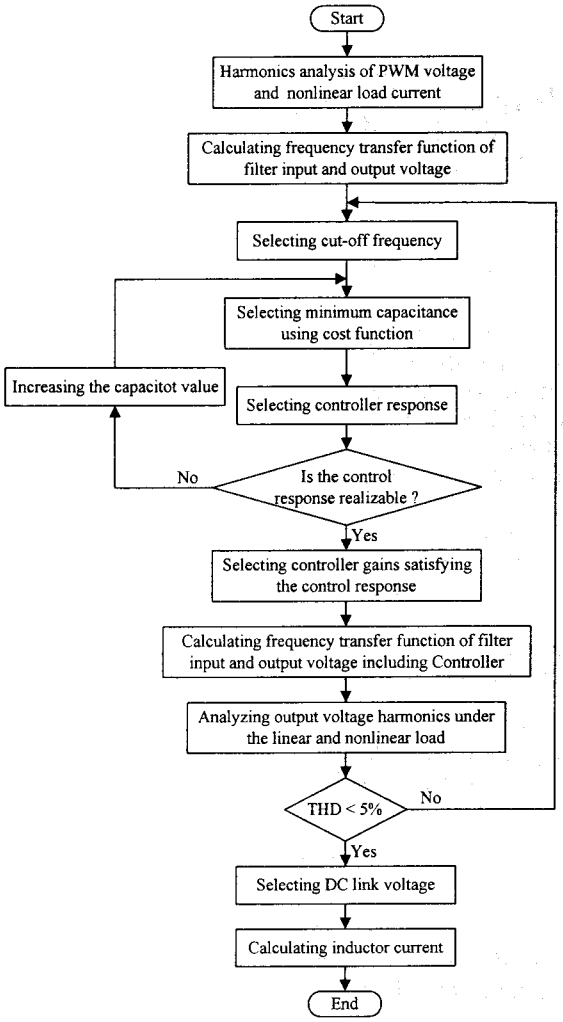


Fig. 4. Flowchart of filter design method.

1) The input voltage waveform of the filter is ideally same as the output waveform of the sinusoidal PWM-VSI.
2) The filter has no loss.
3) Each of the fundamental RMS value of the rated current and the rated voltage of the filter output is 1.0[p.u]

B. Output filter analysis and design method

Fig. 4 shows the flowchart of the filter analysis and design in this paper.

V. FILTER DESIGN

A. Harmonic analysis of input voltage and nonlinear load current

If input voltage of the filter is an ideal SPWM-VSI waveform, the inverter output voltage is presented by multiplying DC voltage and switching function as (8).

$$V_A(\omega t) = V_{dc} \cdot S(\omega t) = V_{dc} MI \sin(\omega_0 t) + V_{dc} \sum_{n=d}^{\infty} A_n \sin(n\omega_0 t) \quad (8)$$

where

d : 1st switching harmonic

MI : modulation index

Fourier coefficients of the input voltage normalized Vdcare listed in Table 1.[7]

Table 1. Normalized fourier coefficients Vn/Vdc for bipolar PWM

Order	MI=1	MI=0.9	MI=0.8	MI=0.7
1	1.00	0.90	0.80	0.70
F_{sw}	0.60	0.71	0.82	0.92
$F_{sw} \pm 2$	0.32	0.27	0.22	0.17

Nonlinear load of the rectifier is fixed for CF to be 3 in an ideal sinusoidal voltage source. The result of FFT analysis for the load current normalized by the fundamentalcurrent is listed in Table 2.

Table 2. Normalized fourier coefficients Vn/Vdc for bipolar PWM

Order	1	3	5	7	9	11
Magnitude	1.00	0.73	0.35	0.07	0.04	0.02

B. Cut-off frequency selection

The cut-off frequency of L-C filter is determined without considering the load current dependent term in (3) and the voltage transfer function is described as (9).

On the assumption that inverter output voltage is an ideal sinusoidal PWM-VSI, (9) is modified as (10). Then the cut off frequency of the filter is selected to attenuate the filter output harmonics to the input harmonics below 3[%].[3]

$$\frac{V_C(j\omega)}{V_A(j\omega)} = \frac{1}{1 - L_f C_f \omega^2} = \frac{1}{\left| n^2 \frac{X_L}{X_C} - 1 \right|} \quad (9)$$

$$\left| \frac{V_C(j\omega)}{V_A(j\omega)} \right| = \frac{1}{\left| n^2 \frac{X_L}{X_C} - 1 \right|} \le 0.03$$

$$33.3 \le n^2 \frac{X_L}{X_C} - 1$$

$$\frac{34.2}{n^2} \le \frac{X_L}{X_C} \quad (10)$$

C. Range selection of capacitor value

The limit value of capacitor is determined from the cost function defined as (11) at the minimum value of the cost function. Considering the reactive power inthe L-C components, the reactive power of inductor is weighted two times higher than that of capacitor in this paper due to the real price[3].

$$COST = \frac{2KVAL + KVAC}{\sum_{n=1,odd}^{n} |V_{on} \cdot I_{on}|} \quad (11)$$

where

$$KVAL = \sum_{n=1,odd}^{n} |I_{on}|^2 X_{Ln}$$

$$KVAC = \sum_{n=1,odd}^{n} \frac{|V_{Cn}|^2}{X_{Cn}}$$

D. System response and calculation of capacitor value

For the analysis of the controller response, the transfer function of filter output voltage to the load current shown in (7) is examined. As shown in (12), the transfer ratio is limited below 1[%]. In this paper, the 5th harmonics is treated to satisfy the above condition after the empirical comparative calculation between 3rd harmonics and 5th harmonics.

$$\left| \frac{V_C(j\omega)}{I_O(j\omega)} \right| = \frac{n^2 \omega_0^2 \tau^3}{12.5 C_f} = \frac{n^2 \omega_0^2 \tau^3 X_C}{12.5} \le 0.01$$

$$X_C \le \frac{0.125}{n^2 \omega_0^3} \tau^3 \quad (12)$$

E. DC Link voltage calculation

The DC link voltage should be determined at the conditionof the smallest MI value, because the amplitude of dominant harmonics is increased as the decrease of MI value. The MI value is decreased as the increase of load power factor. So the DC link voltage is calculated at the rated resistor load in this paper.

With consideration of the ESR of the inductor, the input voltage of the filter is decided by the sum of each fundamental frequency of the capacitor, inductor, and ESR of the inductor. For the appropriate MI

value to calculate the DC voltage, it should not diverge from the linear modulation even though the load fluctuation. Equation (13) shows the proposed calculation of the DC link voltage.

$$V_{dc} = \frac{\sqrt{2}|V_A|}{MI} = \frac{\sqrt{2}\sqrt{\left(V_C - \frac{X_L V_C}{X_C} + \frac{R_f V_C}{Z_L}\right)^2 + \left(\frac{X_L V_C}{Z_L} + \frac{R_f V_C}{X_C}\right)^2}}{MI} \quad (13)$$

F. THD calculation of output voltage

The THD is defined as (14).

$$THD = \frac{\sqrt{\sum_{n=3,odd}^{\infty}(V_{Cn})^2}}{V_{C1}} \quad (14)$$

If the calculated THD is over 5[%] at the linear load, we have to repeat the above process after decreasing the ratio of dominant harmonics in (10) lower than 3[%]. If THD satisfies 5[%] limit at the linear load but dissatisfies at the nonlinear load, we have to repeat the above process after decreasing the ratio of voltage to current transfer ratio in (12) lower than 1[%]. If THD is below 5[%] at the linear and nonlinear load, the design process is over.

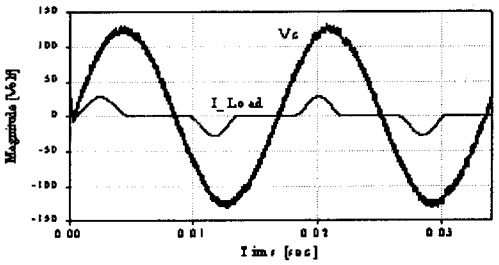
VI. SIMULATION AND EXPERIMENT RESULT

The LC filter designed according to the procedure of the filter design described in section V.

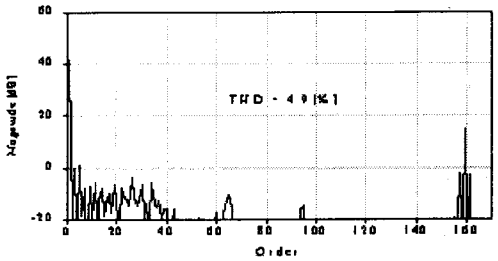
Table 3. Simulation and experiment parameter

Rating Power	2[KVA]	Switching Frequency	9.54[Khz]
Output Voltage	110[V]	System Time Constant	250[us]
Considering The System Time constant	L_f=250[uH]	Considering the cost function	L_f=1450[uH]
	C_f=40[uF]		C_f=10[uF]
	R_f=0.03[Ω]		R_f=0.05[Ω]

The controller is designed by the method of CDM and simulation is performed by ACSL tool after applying the designed values. The parameters for the simulation are listed in table 3.
The simulated and experimental results in the case of increasing the filter capacitance according to the time constant are shown in Fig.3 and Fig. 4. As the results of them, both THDs are under 5% and the both figures of spectrums are same. Fig. 5 and Fig. 6 show the simulation and experimental results respectively after selecting the inductance and capacitance for the minimum cost function mentioned above.
Differently from the same THDs under the linear load, they are little bit different from each other under the nonlinear load. As the controller gains have not been tuned exactly, both THDs are different. But both harmonics distributions are almost same.



(a) Output voltage and load current waveforms



(b) Harmonic spectrum of output voltage.

Fig. 5. Simulation results under rectifier load with CF=3 using the system time constant

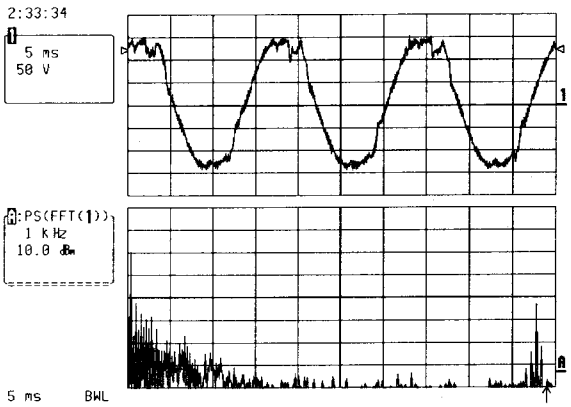
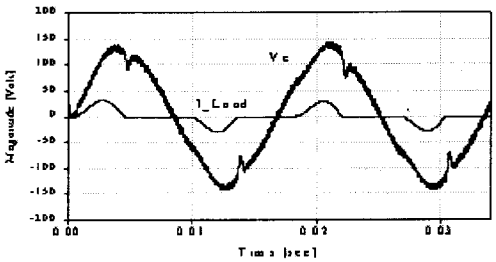
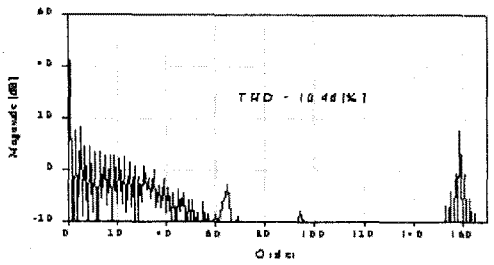


Fig. 6. Experimental results under rectifier load with CF=3 using the system time constant
Upper: Output voltage and load current waveforms.
Lower: Harmonic spectrum of output voltage.



(a) Output voltage and load current waveforms.



(b) Harmonic spectrum of output voltage.

Fig. 6. Simulation results under rectifier load with CF=3 using the cost function.

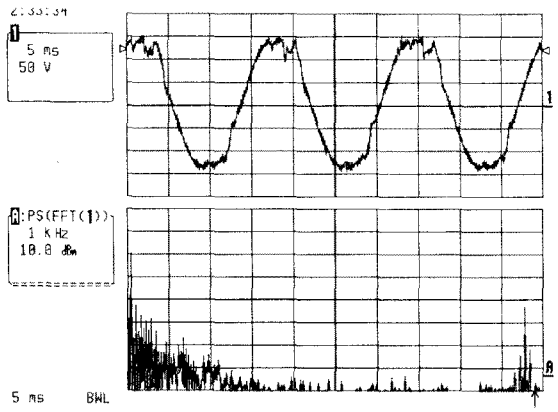


Fig. 7. Experimental results under rectifier load with CF=3 using the cost function.

Upper: Output voltage and load current waveforms.

Lower: Harmonic spectrum of output voltage.

VII. CONCLUSION

This paper describes a study on the output filter design of the single phase PWM-VSI considering the response of controller. To overcome the problem of conventional filter design technique, which is done without controller, the transfer function of UPS output voltage to the load current with a time constant including the filter capacitance and the control response is driven. The amplitude of dominant switching harmonics and the low order voltage harmonics caused by the nonlinear load current is given initially 3[%] and 1[%] respectively. To confirm the validity of design value, the simulation of filter design procedure is done. If there any fault not satisfying the limit of 5[%] THD due to the harmonics neglected during the calculation, we repeat the design procedure after decreasing the initial value of the amplitude of dominant switching harmonics and the low order voltage harmonics till satisfying the THD limit.

Using the design procedure of L-C low pass filter for PWM-VSI proposed in this paper, we can determine the L-C filter value without using any try and error method used conventionally when we design the system controller. The validity of this proposed technique is well verified through the simulation and experimental results.

VIII. REFERENCES

[1] A. Kusco and D. Galler, "Output Impedance of PWM UPS Inverter- Feedback VS. Filters, " in Conf. Rec. IEEE PESC'90, pp. 1044-1048, 1990.

[2] M. Boost and P. Ziogas, "Towards a Zero-Output Impedance UPS system, " IEEE Trans. Ind. Appl., vol. 25, no. 3, pp. 408-418, 1989.

[3] S. B. Dewan and P. D. Ziogas, "Optimum Filter Design of a Single Phase Solid-State UPS System", IEEE Trans. Ind. Appl., vol. IA-15, no. 6, pp. 664-669, 1979.

[4] S. B. Dewan, "Optimum Input and Output Filters for a Single Phase Rectifier Power Supply", IEEE Trans. Ind. Appl., vol. IA-21, no. 3, pp. 282-288, 1981.

[5] J. Kim and J. Choi, " Robust Control of Single Phase UPS InverterUsing Coefficient Diagram Method," in Conf. Rec. of KIEE Power Electronics, pp. III-A-11-15, 2000.

[6] S. Manabe, "Coefficient Diagram Method," 14th IFAC Symposium on Automatic Control in Aerospace, pp. 199-210, 1998.

[7] D. W. Hart, Introduction to Power Electronics, Prentice Hall, pp. 312-317, 1997.