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# Switching Issues for High Density MRAM

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Successful demonstrations by the previous studies ensure that MRAM technology is a strong candidate of universal memory among the other new memory technologies from the viewpoints of power consumption, speed, scalability, retention, endurance, and density. However there are still some fundamental issues to be solved to realize density requirement that is attributted to small switching margin in the core array consisting of sub-micron or deep sub-micron magnetic tunnel junction (MTJ) cells[1].

In a MRAM array, the conventional writing operation uses a half selection scheme that induces a magnetic field simultaneously by two orthogonal line currents on a specific cell. However some cells selected by only one current line, Digit line (D/L) or Bit line (B/L), are partially or fully switched, which cells acts as a fail bit in the array. This writing scheme is directly related to the low writing current margin due to asteroid distribution.

In this study, we consider the technological issues to improve the writing margin in sub-μm MRAM array, such as low Ms free layer, Synthetic anti-ferromagnetic (SAF) free layer and ultra-smooth roughness of bottom electrode. A new switching architecture without digit line current, which uses a local magnetic field generated directly by the current flowing at bottom electrode, is also proposed.

1. Taewan Kim, et al, J. of Magnetism. and Magnetic. Materials. **282**, 232-236 (2004)