Advances in Package-on-Package Technology for Logic + Memory Integration

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Package on Package Technology

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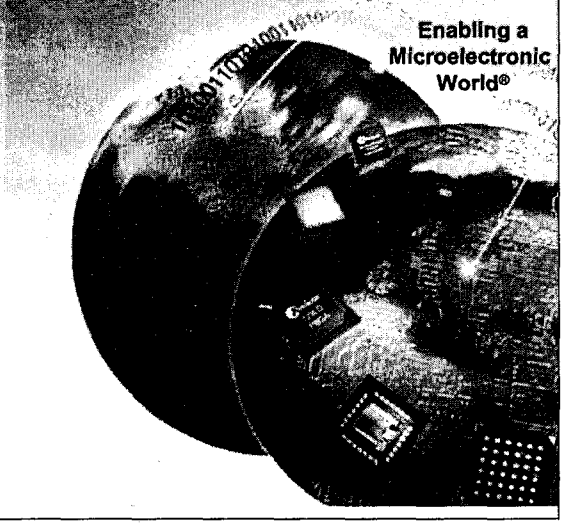
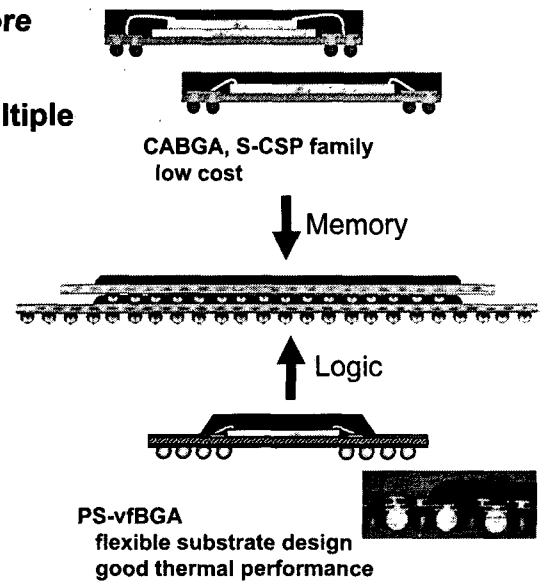


Amkor Technology®

Package-on-Package Benefits

- **Higher final test yield because each package in stack is tested before final assembly**
- **Easier to integrate die from multiple suppliers**
  - Eliminates margin stacking
  - Simplifies supply-chain model
- **OEM controls supply chain**
  - Stacking during board mount
  - Can dual source memory
  - Easily change memory density
- **FA is simplified**
- **Ideal for logic plus memory integration**



Baseband + Memory Integration without cost / supply penalties

Source: Web-Feet Research	2003 $ Bn	2007	CAGR
Flash (internal)	$2.9	$5.7	18.4%
Flash Card (ext)	$0.2	$2.8	93.4%
Mobile DRAM	$0.2	$2.1	77.8%
SRAM	$0.8	$1.4	15.0 %
Total	$4.1	$12.0	30.8 %

Source: IDC	2003 $ Bn	2007	CAGR
App/ Integrated Proc	$0.6	$2.5	42.9 %
BB Processor	$5.1	$6.5	6.3 %
MM Co-Proc	$0.2	$0.3	10.7 %
Total	$5.9	$9.3	12.1 %
Memory + Proc Total	$10	$21.3	20.8 %

BB & Memory architecture thrusts

- Cost reduction focus across segments
- Integration - size & cost reduction in Smart & 3G phones
- NOR to NAND for higher density and lower cost / MB
- SRAM to Mobile DRAM for higher speed & density at lower cost

- SCSP (SiP), PoP, PiP main BB pkg options for memory integration
  - PoP has strongest support across supply chain as can provide lowest cost of ownership and greatest sourcing flexibility

Integration Challenge

Optimize for: Size / Cost Reduction / Supply Flexibility

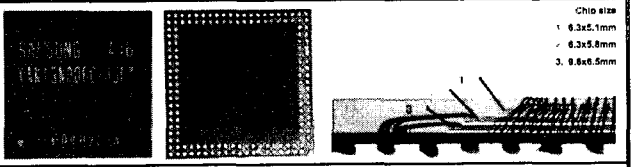
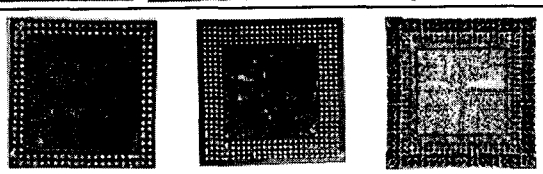
- Goal shrink Bband section w/ 144mm² area as target for logic + memory integration - to facilitate broader form factor flexibility and higher feature integration
- Semiconductor content forecast:

Function	2003	2008	CAGR	% of 2008 Content
Bband	$15.90	$20.20	4.8%	42%
Memory	$9.30	$12.70	6.5%	27%
RF, other	$18.00	$15.00	-3.6%	31%

Source: *iSuppli*

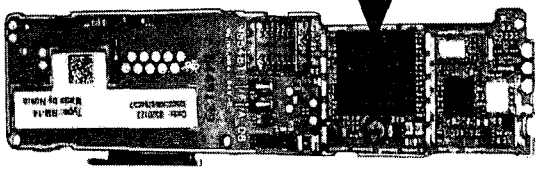
- 2600 different handsets now on the market, 1300 new models in 2004 alone challenging design / flexibility
  - Higher risk of missing service provider design win.
- Need logic + memory architecture that allows increasing memory capacity late in phone launch to meet service providers needs at lowest system cost
  - SCSP / SiP seen as limiting Flexibility.

PoP for Mobile Phone – Baseband + Memory

	External size	Appearance of Package (Top view/Bottom view)
Top Package Memory	Package size 14x14x0.99mm Pin count 151pins in 0.65mmP	
Bottom Package Baseband Processor	Package Size 14x14x0.59mm Pin count 353pins in 0.5mmP Chip size: 8.2x8.2mm	

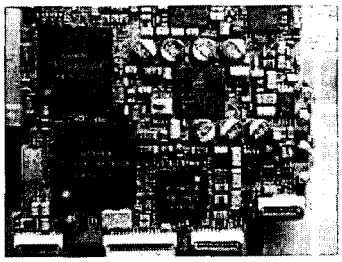
Combination ASIC/DSP package with Memory package
SRAM and Flash memory and Graphic DDR

Nokia 7280



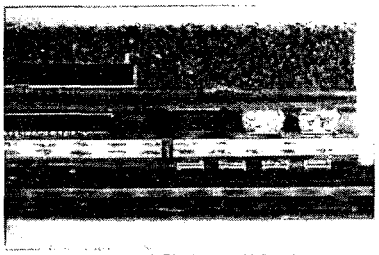
PoP Bottom Package Assembled by Amkor Source: SemiConsult 2005

Sony T-1 Cybershot DSC



The bottom package is a 14mm x 14mm flip-chip-on-rigid CSP. Unusually, the package's 304 I/O are LGA pads that are arranged in four peripheral rows with a 0.5mm pitch. The collapsed package height was measured as 0.6mm.

SONY/SHINKO PoP BOTTOM PACKAGE
2 photos



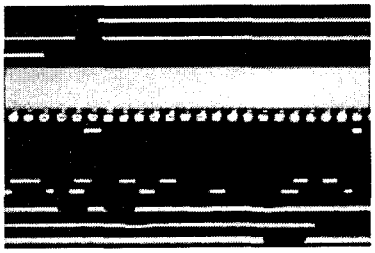
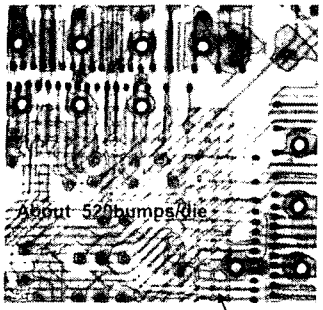
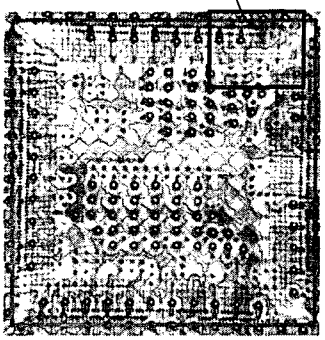


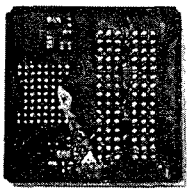
Photo Source: Prismark/Binghamton University

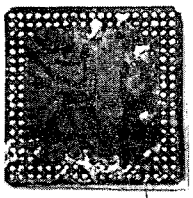
An Example of PoP for DSC Use in Japan



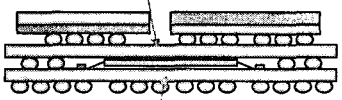


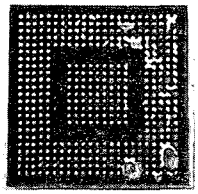
<Top view> <Bottom view>

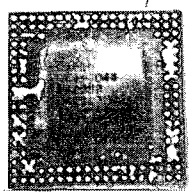




Die size	7x7x0.165
Substrate	0.457mm t 1/2/1 build up
Interposer	0.23mm t







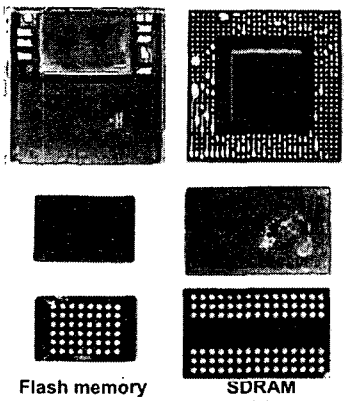
<Top view> <Bottom view>

Source: SemiConsult 2005

An Example of PoP for DSC Use in Japan

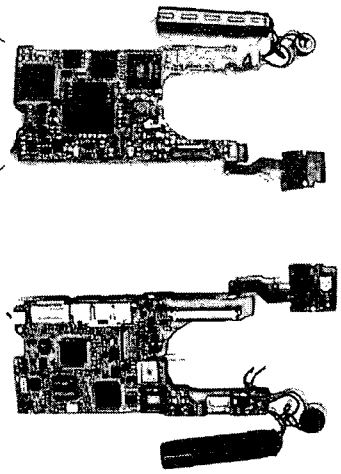
Graphic Engine Module

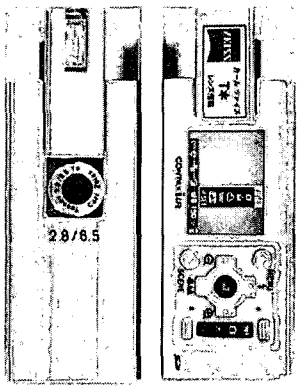
MCM
15x15x1.8mm
Bottom:
Graphic Engine
FCBGA 481pins
15x15x0.65mm



Flash memory
FBGA 48pins
9x6xx1.2mm

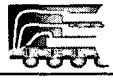
SDRAM
FBGA 90pins
13x8x1.4mm



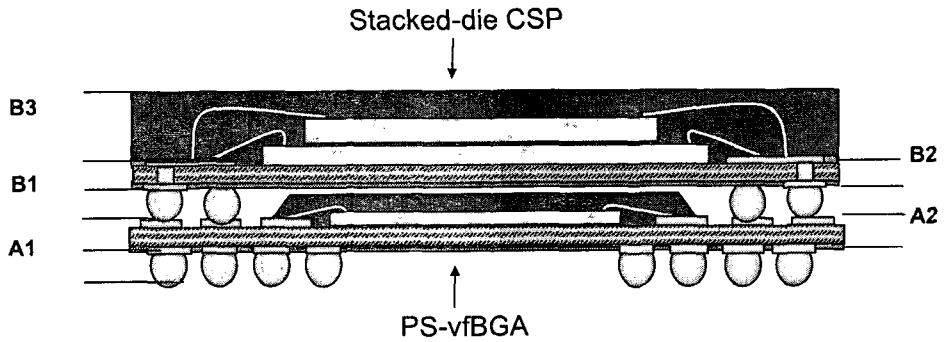


Source: SemiConsult 2005

Memory Integration - Miniaturization Options

Package Options	CSP + MCP 	Stacked CSP (SiP) 	PoP 
Logic Pkg	10x10mm CSP 0.4mm pitch	12 x 12 to 13 x 13mm SCSP	14x14mm PSvfBGA (12mm w/ 128 IF)
Memory Pkg	8 x 10 to 8 x 12mm MCP	Wafer supply business Test support	14x14mm top PoP 12x12mm w/ 128 IF)
PWB Area	216mm² (worse case w/ 2mm between)	169mm² to 144mm²	196mm² roadmap to 144mm²
System Cost	Lowest	Highest	Good
Thermal perf.	Best	Worse	Good
Elect perf.	Good	Poss. best	Risk if poor co-design
Total Z height	1.2mm – 1.0mm	1.4mm – 1.2mm	1.6 to 1.5mm
Sourcing Flexibility	Will be best following 0.4mm CSP qual.	Worst	Good

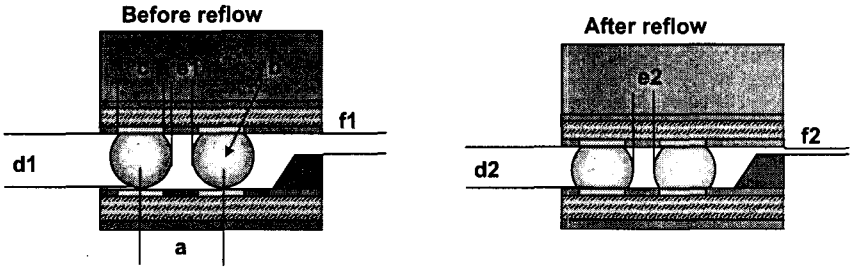
PoP Package Construction



Symbol	unit	SCSP + PS-vfBGA Min	Max	Nom
A1 (Ball, 0.5 pitch)	mm	0.200	0.300	0.250
A2 (4L laminate)	mm	0.260	0.340	0.300
B1 (Ball, 0.65 pitch)	mm	0.270	0.330	0.300
B2 (2L laminate)	mm	0.180	0.240	0.210
B3 (Mold cap)	mm	0.420	0.480	0.450
Overall Pkg height	mm	1.428	1.592	1.510

PoP Top Package Stand-off Height

- **Based on the experimental results, larger solder ball is suggested for high stacking yield**
  - 0.33 mm diameter for 0.5 mm pitch top package
  - 0.42~0.45 mm diameter for 0.65 mm pitch top package

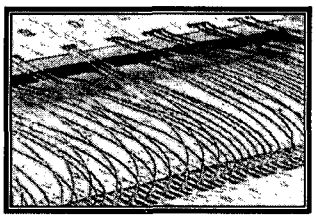


a	b	c	d1	e1	d2	e2	f1	f2	Stacking
0.5	0.33	0.25	0.28	0.17	0.22	0.17	0.08	0.02	100%
0.5	0.3	0.22	0.25	0.20	0.21	0.20	0.05	0.01	95%
0.5	0.3	0.25	0.24	0.19	0.18	0.19	0.04	-0.02	0%
0.65	0.42	0.30	0.36	0.23	0.30	0.23	0.09	0.03	100%

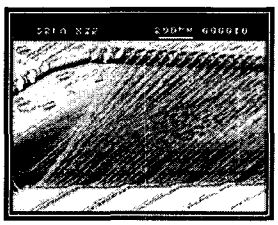
The numbers of a-f are nominal or calculated value. All failure at stacking were open failure.

PoP Wirebonding – Low Loop Formation

- **Low loop wirebonding to support thin package applications**
- **SSB & Wedge Bonding - low loop application to thin die**
  - low loop less than 3 mil in production
  - No wire cross among wires bonded on same die
  - Bonding priority: Ball bonding > SSB > Wedge
    - Bond pad size: 70um long (wedge)



SSB(Reverse) Bonding

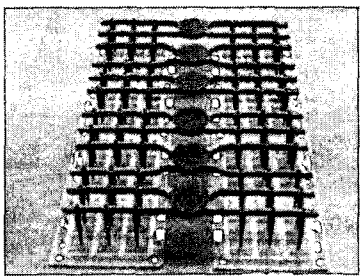


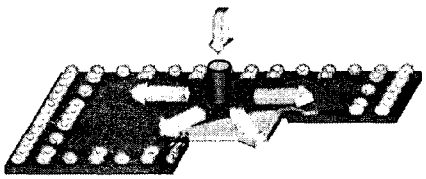
Wedge Bonding

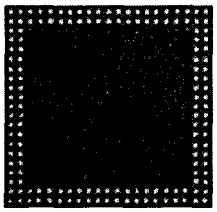
Note) Wedge bonder is available at R&D only. Very limited support at this time.

Center Pin-Gate Mold

Cavity gating is from center of package







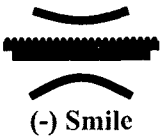
Fills cavity from center

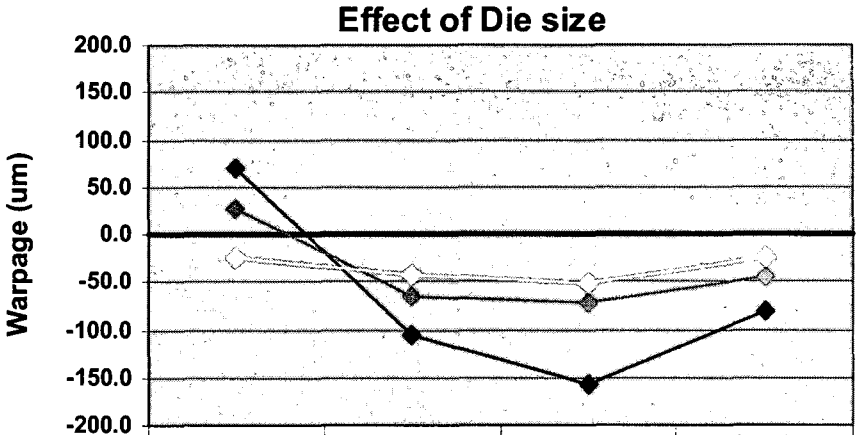
- No gate area needed on package substrate
- Mold flow parallel to wire bonds minimizes wire sweep
- Mold flow from center of array package towards side vents reduces entrapped air and voiding
- Allows very thin mold cap without voiding or incomplete fill
- 0.27 mm mold cap thickness is qualified

Manufacturing Challenge: Controlling Package Flatness

- **Excessive package warpage can cause yield loss during final assembly of the PoP packages to the motherboard.**
- **Package flatness must characterized from room temperature to maximum reflow temperature.**
- **Base package and top package should have similar warpage throughout the reflow profile to ensure good solder joint formation**
- **Key factors affecting package warpage include:**
  - Mold compound CTE, modules and rate of cure shrinkage
  - Die Size
  - Substrate material properties and thickness

PSvfBGA Warpage – 14 mm body

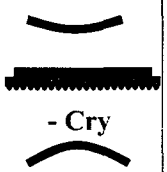


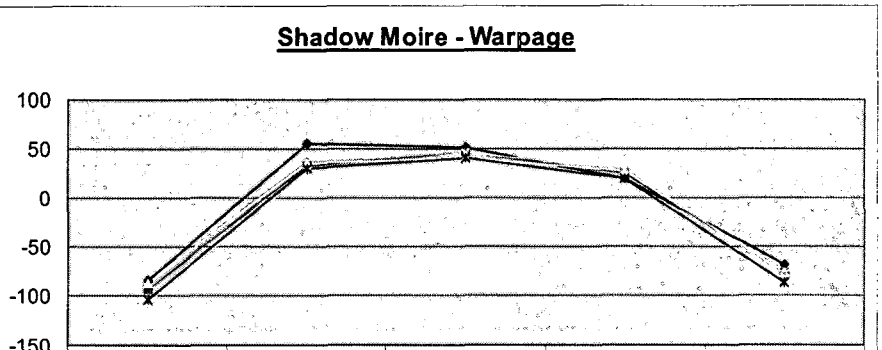


	25'C	183'C	260'C	183'C
8.90 mm	69.8	-104.8	-156.4	-81.2
7.62 mm	27.8	-65.8	-71.6	-44.2
6.35 mm	-24.4	-41.8	-52.0	-25.6

SS : 5 units / plot

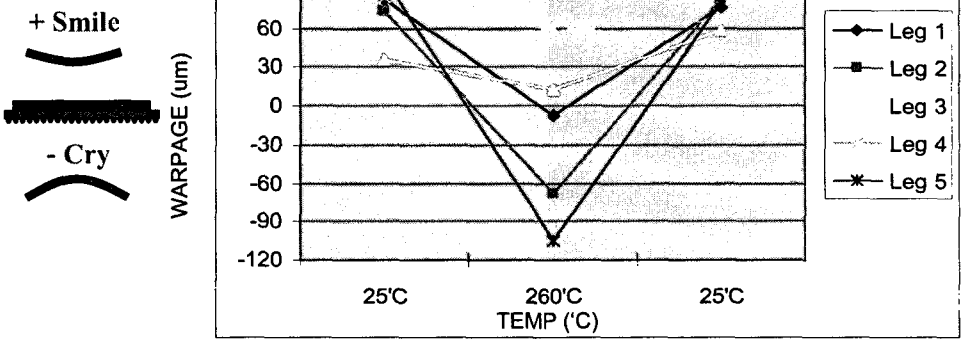
Amkor 12mm Bottom Package – Shadow Moire





	25	183	260	183	25
#1	-83.82	55.88	50.8	20.32	-68.58
#2	-93.98	33.02	45.72	25.4	-76.2
#3	-86.36	35.56	40.64	27.94	-76.2
#4	-106.68	27.94	45.72	30.48	-78.74
#5	-104.14	30.48	40.64	20.32	-86.36

Amkor 14mm Top Package Warpage Optimization

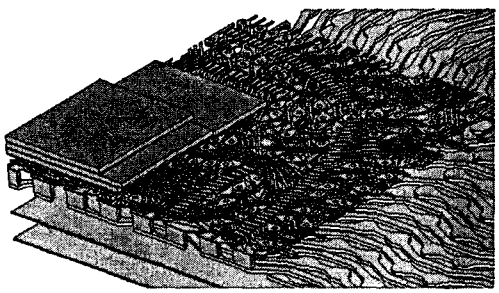


Leg 5 is standard material set, leg 4 chosen for top PoP.
Top and Bottom package have similar smile warpage at 260C

Thermal Performance Comparison
PoP vs. Stacked die CSP

PSvfBGA and SCSP configuration:

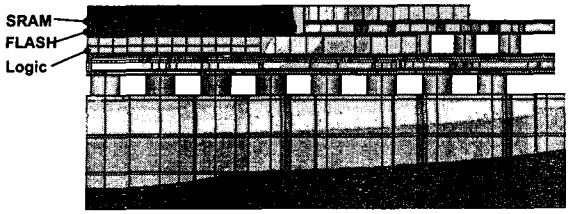
- Body Size: 13.0mm x 13.0mm
- Die 1: 4.94mm x 5.33mm
- Die 2: 5.65mm x 7.95mm
- Die 3: 4.48mm x 5.08mm
- Bottom BGA Array: 225 I/O at 0.80mm pitch
- 70 C Ambient, 0.9W total power

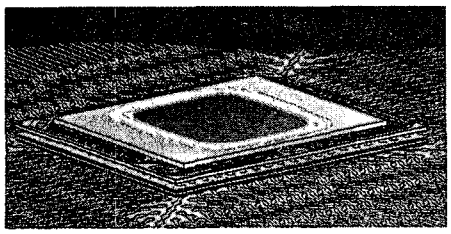


SCSP

PSvfBGA

Thermal Performance Comparison PoP vs. Stacked die CSP





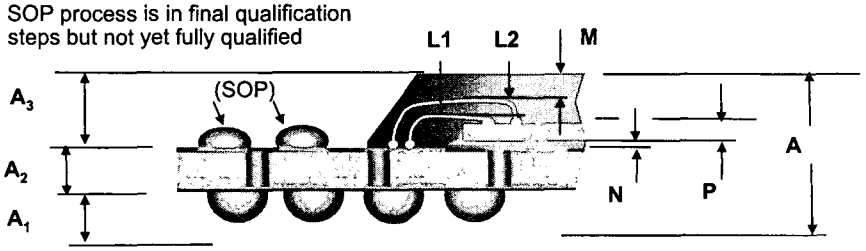
S-CSP and PSvfBGA show similar thermal characteristics

Air velocity (m/s)	Package Style	Die temperature(°C)			Theta-ja (°C/W)	Theta-jb (°C/W)	Theta-jc (°C/W)
		Flash	SRAM	Logic			
0.0	S-CSP (MCP)	94.9	96.9	98.8	32.0	21.2	7.6
1.0		92.6	94.6	96.4	29.4		
2.5		91.7	93.7	95.5	28.4		
0.0	PS vfPBGA	97.8	98.1	95.3	31.3	19.6	11.4
1.0		94. 3	94.6	92.0	27.4		
2.5		93.0	93.2	91.0	25.7		

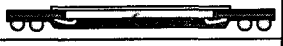
2 Die / 2 Tier PSvfBGA Stack up Details

- **0.35 mm (A3) mold height required for high density die stack or 2 tier wire bond clearance**
- **Solder on pad (SOP) with stnd 0.42mm top ball or larger 0.5mm dia. will be necessary for 0.35mm mold cap clearance**
  - Best SOP ball size demonstrated to be between 0.2 ~ 0.3 mm to stack 0.65 mm pitch memory package above 0.35mm mold cap
  - Risk of ball bridging at 0.65mm pitch with larger ball needs to be studied vs SOP option
  - SOP process is in final qualification steps but not yet fully qualified

Description		0.35mm mold cap PSvfBGA		
		Min	Max	Nominal
Loop Height (L1)	(mm)	0.075	0.075	0.075
Loop Height (L2)	(mm)	0.075	0.075	0.075
Adhesive (N)	(mm)	0.025	0.025	0.025
Die Thickness (P)	(mm)	0.075	0.100	0.075
Mold Cap Clearance (M)	(mm)	0.075	0.075	0.100
Mold Cap Thickness (A_3)	(mm)	0.320	0.380	0.350
Substrate Thickness (A_2)	(mm)	0.260	0.340	0.300
Ball Height, post reflow (A_1)	(mm)	0.180	0.280	0.230
Pkg Total Height (A) *	(mm)	0.800	1.000	0.880



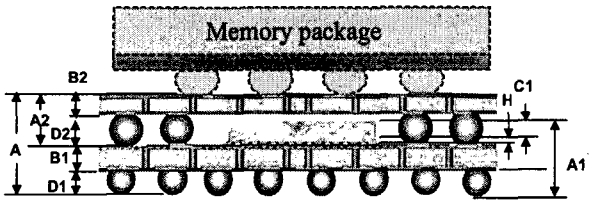
PoP Base Package Reliability Results

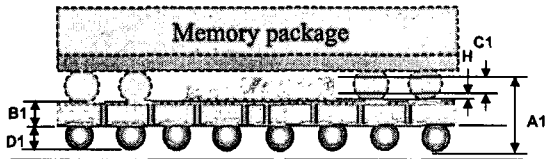
Base Package Type	MRT 260°C (+0/-5) JEDEC	T/C -55 °C / 125 °C 1000 cycles	T/H 85 °C / 85 % 1000 hrs	HTS 150 °C 1000 hrs	HAST 130 °C / 85 % 96 hrs
etCSP 176, 12BD, 0.55t, 7.62sq die 	L1, 3x, 0/66	0/228	0/228	0/228	0/135
SetCSP 176, 12BD, 0.7t, 6.35sq+7.62sq die	L1, 3x, 0/22	0/77	0/77	0/77	0/51
SetCSP 176, 12BD, 0.55t, 6.35sq+7.62sq die 	L3, 3x, 0/22	0/76	---	0/76	0/76
PSetCSP 352, 13BD, 0.75t, 7.62sq die 	L1, 4x, 0/22	0/76	0/76	0/76	0/45
etCSP 72, 13x11BD / PSetCSP 352 13BD stacked	---	0/76	---	---	---
PSvfBGA 352, 14BD, 0.90t, 7.62sq die 	L3, 4x, 0/22	0/76	---	0/76	0/76

Flip-chip PoP Base Package

- **POP package size reduction**
  - –1~3mm size reduction with Au stud bump
- **Electrical performance**
  - – No IR drop impact with low K die
  - – High frequency
  - – Less electrical noise
- **0.5mm pitch Top package possible**
  - – More I/Os per sq mm
  - – More functions per sq mm
- **Lower POP height**
  - – no interposer
  - – no encapsulation
- **Room to put passive components & IC with interposer**
  - – SiP Module possible
  - – Best area utilization

PSfcBGA overview - interposer optional





Description	unit	PS-fcBGA with Interposer			without interposer		
		Min	Max	Nom	Min	Max	Nom
H (FC bump)	mm	0.055	0.075	0.065	0.055	0.075	0.065
D1 (Ball, 0.5 pitch)	mm	0.180	0.240	0.210	0.180	0.240	0.210
D2 (Ball, 0.65 pitch)	mm	0.280	0.340	0.310	0.280	0.340	0.310
C1 (Flip chip)	mm	0.192	0.208	0.200	0.192	0.208	0.200
B2 (2L laminate)	mm	0.170	0.250	0.210	NR	NR	NR
B1 (4L laminate) *	mm	0.220	0.300	0.260	0.220	0.300	0.260
A2 (Interposer stand off)	mm	0.470	0.570	0.520	NR	NR	NR
Bottom(PS-fcBGA) package (A1)	mm	0.697	0.773	0.735	0.683	0.787	0.735
Package Overall Height (A=A2+ B1+D1) **	mm	0.919	1.061	0.990			

Note) * : *Values for min/max shown are calculated using Root Mean Square (RMS) deviation*

PS-fcCSP - Interposer optional

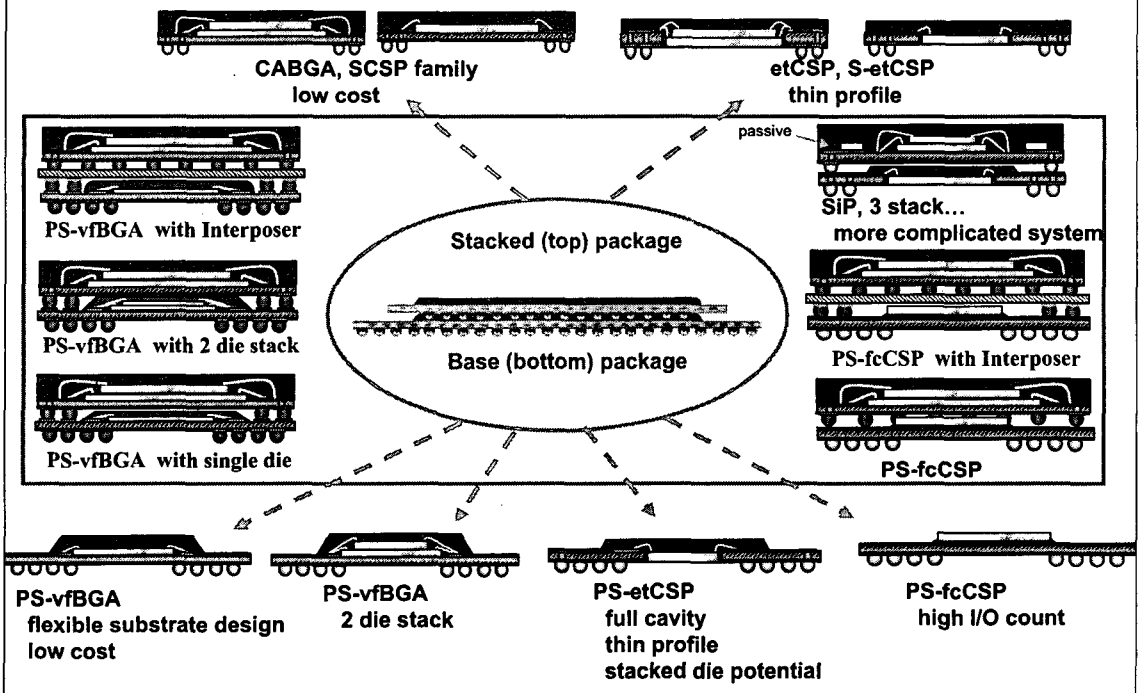
	With interposer	Without interposer
PROS	Free to pick top Package foot print Flexible to select memory pkg Less overall package price Less package warpage Top pkg mounting better & easier Guard FC die More area to put passive & IC	Least overall POP height Simplified process Lower bottom package cost
CONS	Overall POP height Additional Packaging cost Longer electrical path More SB joint	Custom foot print Higher top package price FC die protection against handling

Interposer is optional depending on POP application.

PS-fcCSP Reliability

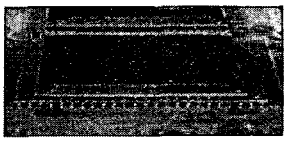
- Internal development
  - 13x13mm, 320 balls, 4 layer substrate
  - FC die : 6.4x6.4mm, 200um bump pitch, lead free
  - MRT : Pass Jedec L3@260'C
    TC : Pass 1,000X (-55/125'C)
- Alpha customer
  - 12x12mm, 201 balls, 2 layer substrate
  - FC die : 5x5mm, 200um bump pitch, lead free
  - MRT : Pass Jedec L3@260'C
    TC : Pass 1,000X (-55/125'C)
    uHAST : 192hrs

PoP Variants



PoP Package Stacking Process Flow

- **SMT-stacking (during board assembly) ... *Amkor's recommendation***
  - Base package is mounted on board with other components
  - Stacked package is flux dipped, then mounted on base package
  - Reflow



- **Pre-stacking (unit-to-unit, then on board)**
  - Bottom package is placed into jig
  - Top package is flux dipped, then mounted on bottom package
  - Reflow
  - Board assembly

	Single Package	SMT-stack	Pre-stack
Packaging	✓	✓	✓
Top package flux & place	↓	↓	✓
Reflow			✓
PWB screen print	✓	✓	✓
Package mount	✓	✓(bottom)	✓
Top package flux & place	↓	✓	↓
Reflow	✓	✓	✓

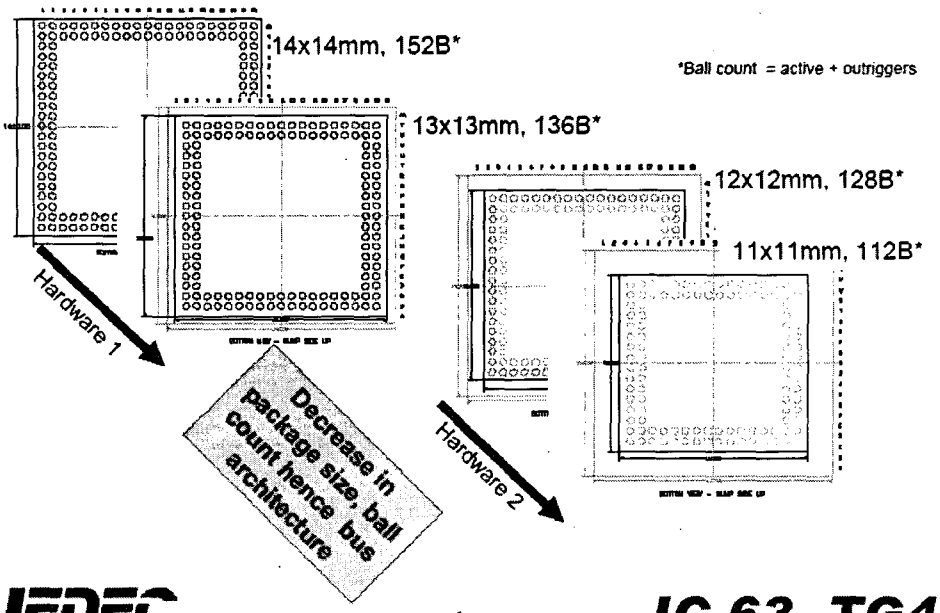
JEDEC Standards

- **JC-11 (Design and Mechanical)**
  - Amkor teamed with Spansion to create PoP Design Guide covering top and bottom packages to ensure mechanical integrity.
    - Covers 8mm to 21mm body sizes.
  - Amkor has received JEDEC approval for 12, 13 and 14mm PSvfBGA mechanical outlines to be registered following Design Guide approval.
- **JC-63 (Pin-outs)**
  - Amkor member of TG4 working group responsible with developing PoP memory interface pin-outs.
  - Intel, Spansion, Sharp and Amkor developed initial pin-out optimization methodology.
    - Wide range of IDMs (mainly memory) now active in TG4
    - 12 and 13mm body sizes had 1st showing ballot

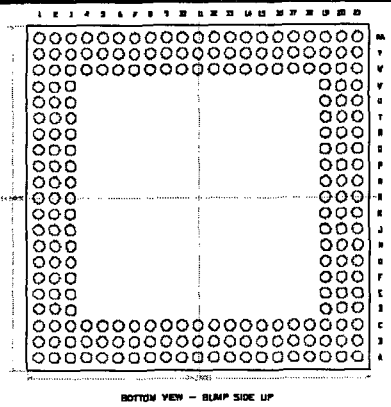
PoP Standardization

- **Memory bus configuration defined by:**
  - Body size and ball pitch
  - Types of memory in combination – NOR, PSRAM, NAND, DRAM
  - Desired bus architecture – Shared bus, single or multiple split bus.
- **Each ball out should handle several memory configurations**
- **When possible test hardware should be shared**
- Sequential order for data and address buses will benefit logic device floor plans for memory interface design.

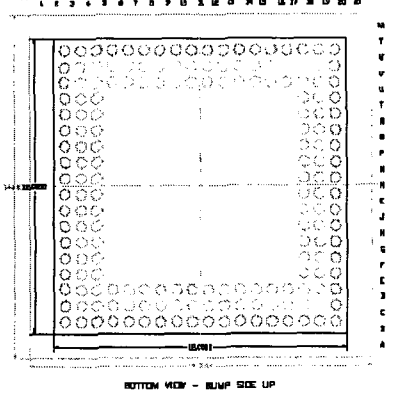
Ballout Scalability



Universal Test Hardware for PoP



BOTTOM VIEW – BUMP SIDE UP



BOTTOM VIEW – BUMP SIDE UP

Hardware 1
Total Ball count: 226B
Package size supported: 14x14 and 13x13

Hardware 2
Total Ball count: 180B
Package size supported: 12x12 and 11x11

Advantages of sharing of hardware:
1. **Lower test cost**
2. **Faster time to market**

2B12D – NOR+PSRAM+NAND+SDRAM

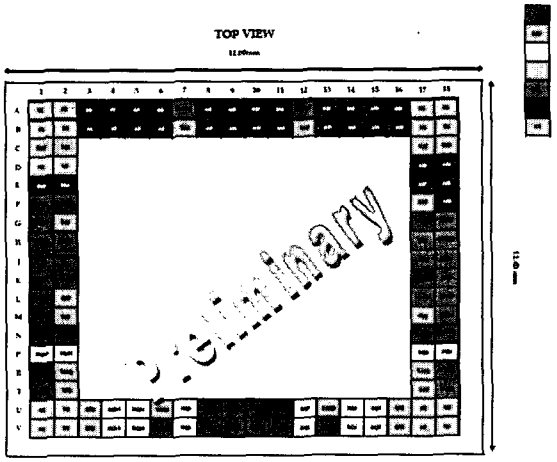
PoP Look-Ahead Pinouts Compilation

Bus Support 4/25 (x16 Nor + x16(p)SRAM + x16 SDRAM + x16 NAND shared database)

12x12 Package Size

2 Perimeters of Balls - 128 Total Balls

TOP VIEW



PoP Summary

- **PoP provides OEMs and EMS with a platform to cost effectively expand options for logic + memory 3D integration**
  - Expands device options by simplifying business logistics of stacking
  - Integration controlled at the system level to best match stacked combinations with system requirements
  - Eliminates margin stacking and expands technology reuse
  - Helps manage the huge cost impacts associated with increasing demand for multi media processing and memory
- **PoP is well timed to enable and leverage:**
  - Mass customization of systems for different use (form, fit and function) requirements
    - Bband and apps processor + memory stack platforms
  - Logic transition to flip chip enables PoP size reduction
    - Area and height reduction
- **Industry standardization is progressing**
- **Amkor provides full turn-key support for base package, memory package and full system integration**