Development of 3D-SiP Including Components in SiP Consortium

Takao Fujitsu

(J-SiP Corporation/Japan)

ISMP2005

Development of 3D-SiP Including Components in SiP Consortium

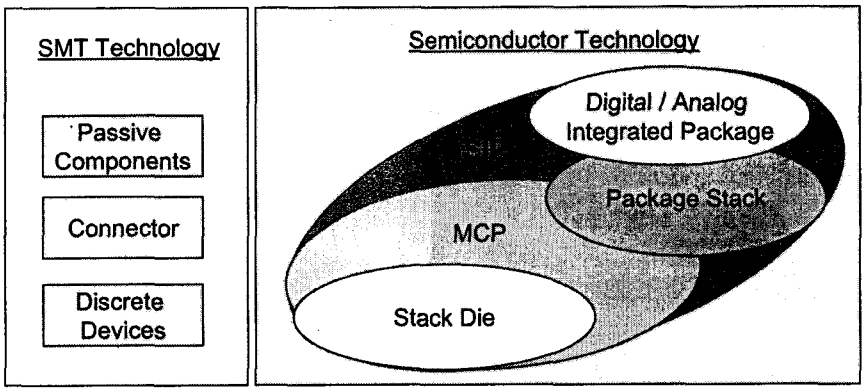
Takao Fujitsu

The chairman of the board
SiP Consortium

President
J-SiP Corporation

SiP CONSORTIUM J-SiP

Current SiP Category



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2D-Jisso to 3D-Jisso

SMT Assembly Infrastructure(Jisso) is getting as mature by current industries standardization.

- Hi Performance and Standardization of Pick & Place Mountor
- Standardization and Finer capability of PCB Design
- Shrink and Standardization of the mount components including semiconductor package

SMT has no big differences in terms of the location (Japan or China)

SMT Infrastructure (fine/small technology) reaches the limitations

SMT well applies 2D Assembly, No good for 3D Assembly

SOC provides additional value as differentiation (SiP as well)

Establish new infrastructure(3D-Jisso) for Fine and Small 3D Assembly by using Semiconductor Packaging Technologies

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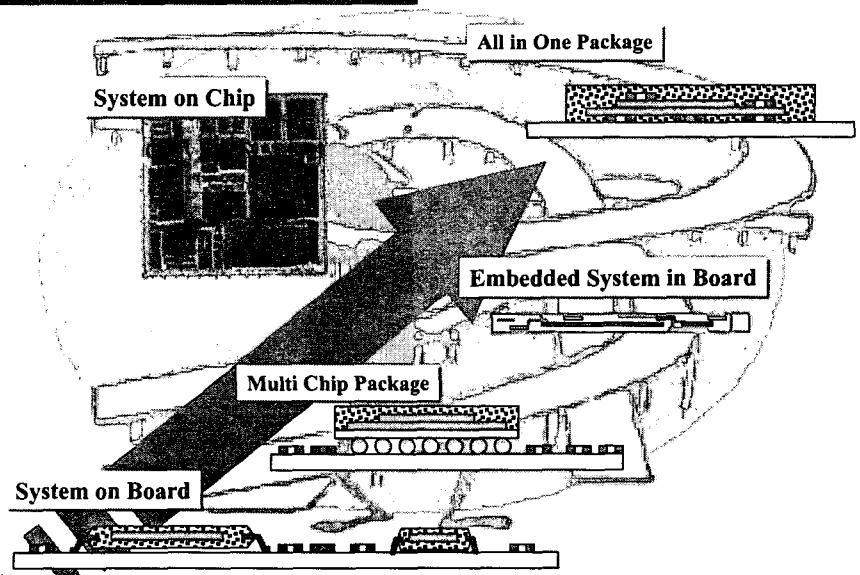
Evolution of System in Package



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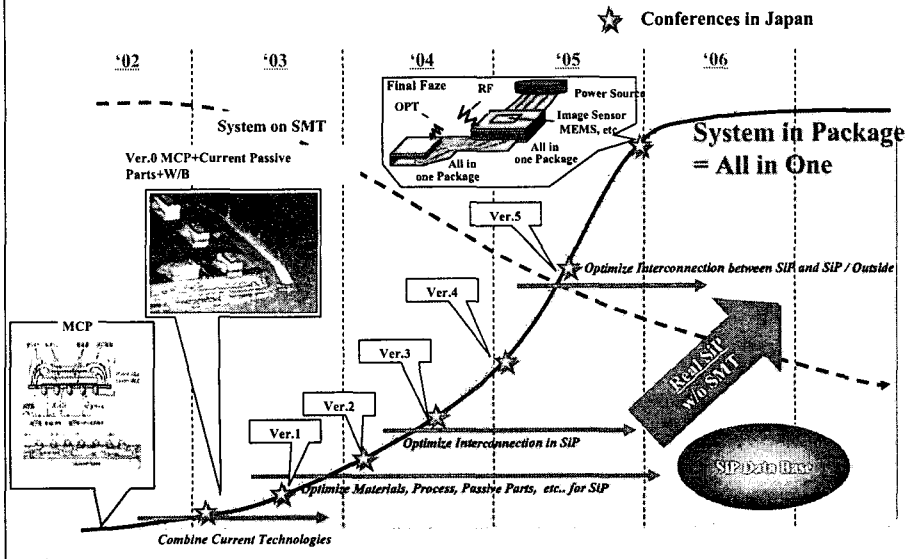
Technology Road Map of SiP Consortium



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SIP Consortium Member

SiP CONSORTIUM

Chairman: Tsuyoshi Kawanishi (TEK Consulting)

Vice Chairman: Tadatomo Suga (Professor, Research Center for Advanced Science and Technology, The University of Tokyo)

The chairman of the board: Takao Fujitsu (President , J-SiP Co.)

Member Companies : J-SiP Co., IBIDEN Co,.Ltd., Sumitomo Bakelite Co,.Ltd., DISCO Corp., Ueno Seiki Ltd., Hitachi Chemical Co,.Ltd., TOPPAN PRINTING CO.,LTD , Nippon Steel Corp, Tanaka Denshi Kogyo K.K., Tomoegawa Paper Co.LTD. LINTEC Corp., SHINKAWA LTD. Renesas Eastern Japan Semiconductor,Inc. Taiyo Yuden Co.,LTD Yamakatsu Denshi Co.

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Plan for 3D-Jisso Infrastructure Development

- Design Technology Development
  - Develop Design Tool for 3D-SiP
- Supply Chain Development
  - Develop and Supply Parts for 3D-Jisso SiP
  - KGD Bare Chip, Components,MEMS parts
- Assembly Technology Development
  - Develop and Promote Packaging Technology by SiP Consortium

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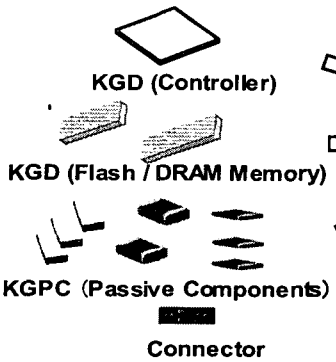
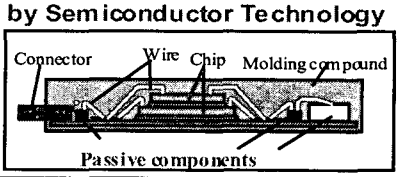
3D-Jisso(All-in-one SiP)

IC / Pasive / etc. → Package Shrinkage / Low Cost



Stack Die / Passive on Board by Semiconductor Technology



Item	SMT (Jisso) Infrastructure	3D-Jisso Infrastructure
Minimum Outer Lead Pitch	0. 4mm	0. 1mm
3D Assembly	NG	3D Wiring
Design Chnage	Re-design substrate	Wire Bond Design Change
Re-work	OK	NG after mold

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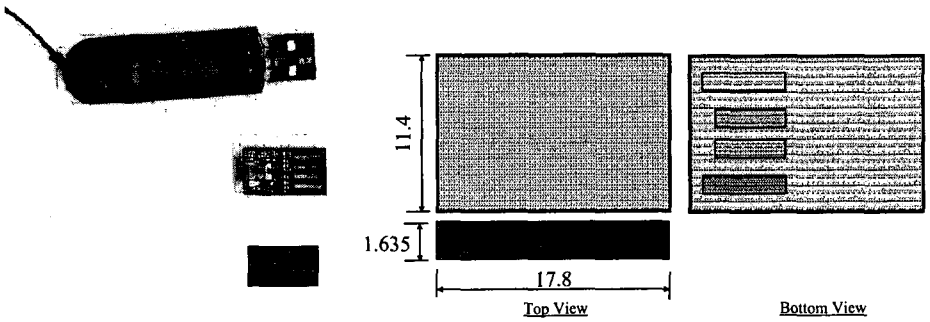
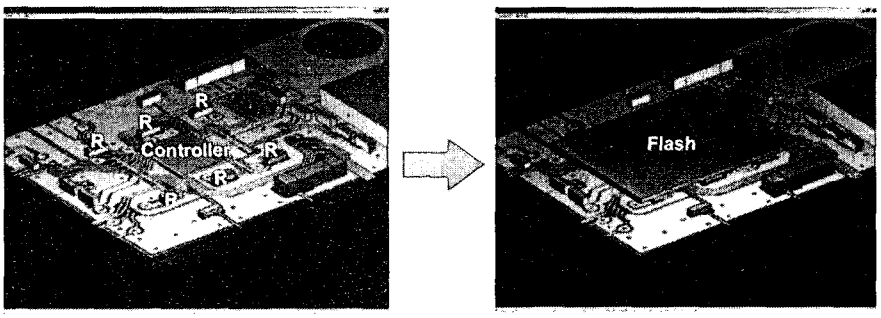
World Smallest USB Pen drive



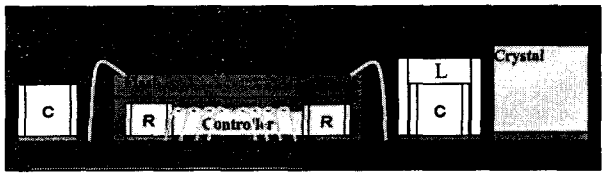
SiP CONSORTIUM J-SiP

World Smallest USB Drive!



Before Flash Chip Stacked

Flash Chip Stacked



Cross Section

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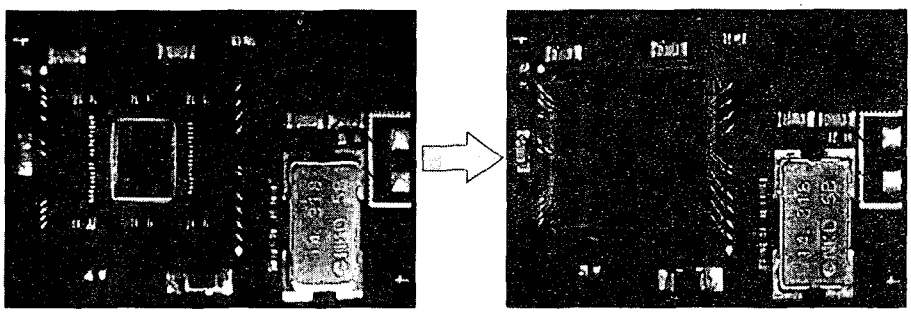
NAND Flash Chip Stacked Sample



Before Flash Chip Stacked

Flash Chip Stacked

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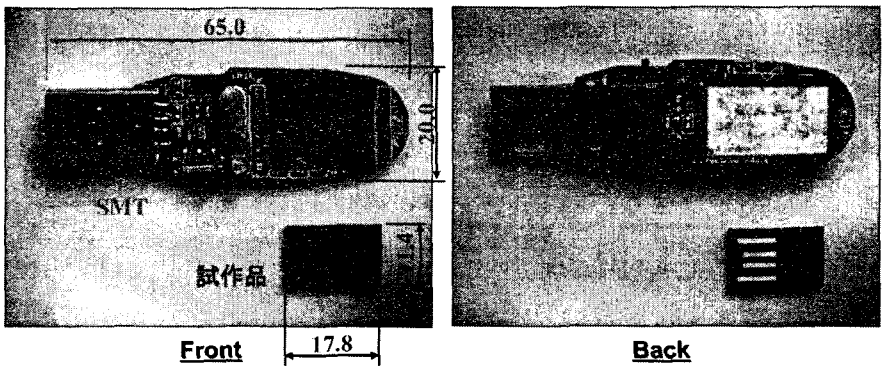
Comparison to SMT Product



Front **Back**

84% Shrink

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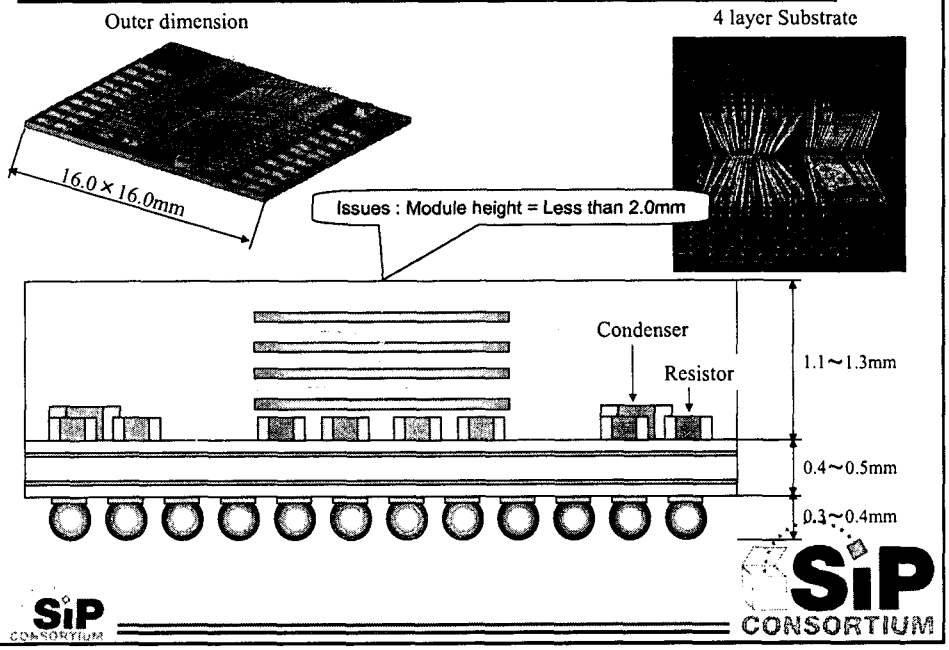
Memory Module Structure and Current Challenges



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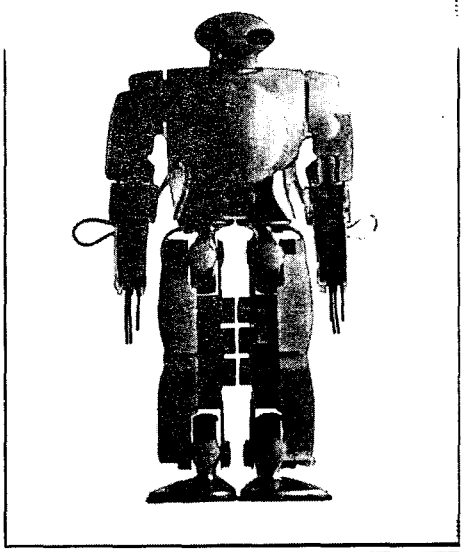
3D-Jisso Application to Humanoid Robot



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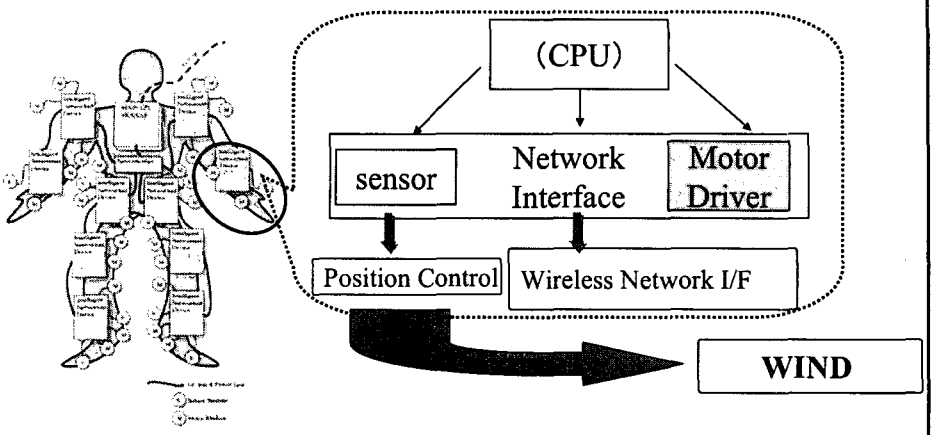
SiP Solution to Humanoid Robot



Small and High Performance Module by SiP

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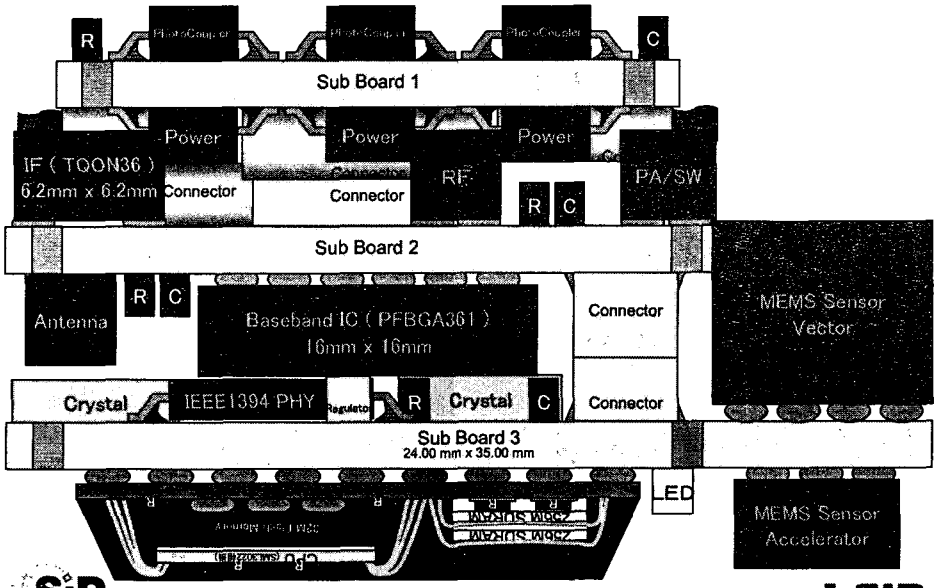
WIND Module



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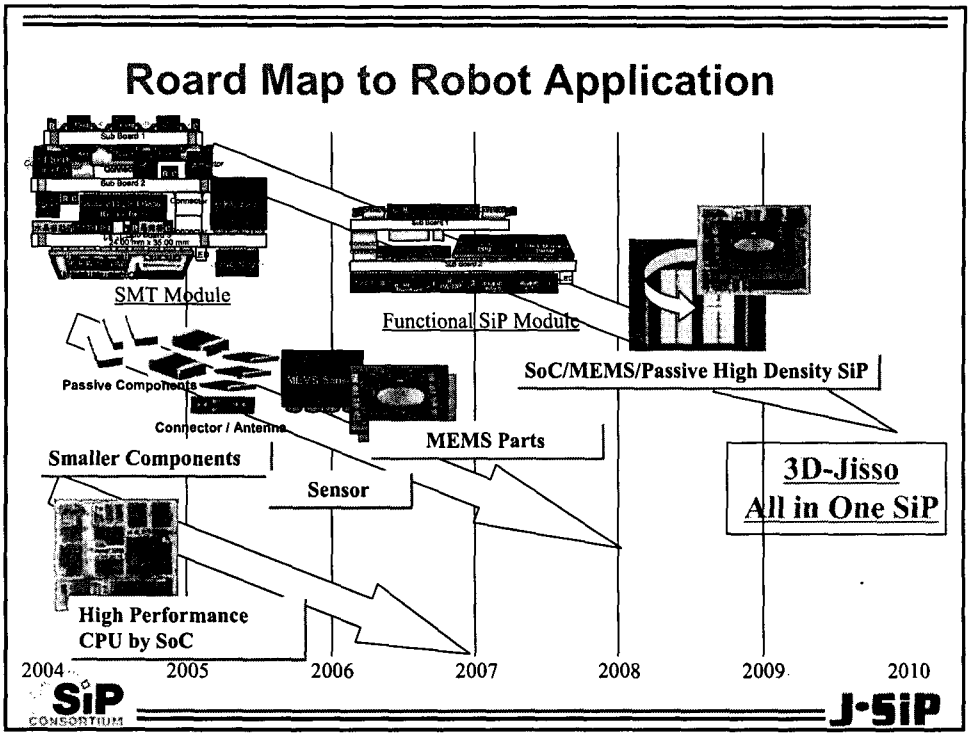
Roard Map to Robot Application
SMT Module
Functional SiP Module
SoC/MEMS/Passive High Density SiP
Passive Components
Connector / Antenna
MEMS Parts
Smaller Components
Sensor
3D-Jisso
All in One SiP
High Performance
CPU by SoC
2004
2005
2006
2007
2008
2009
2010
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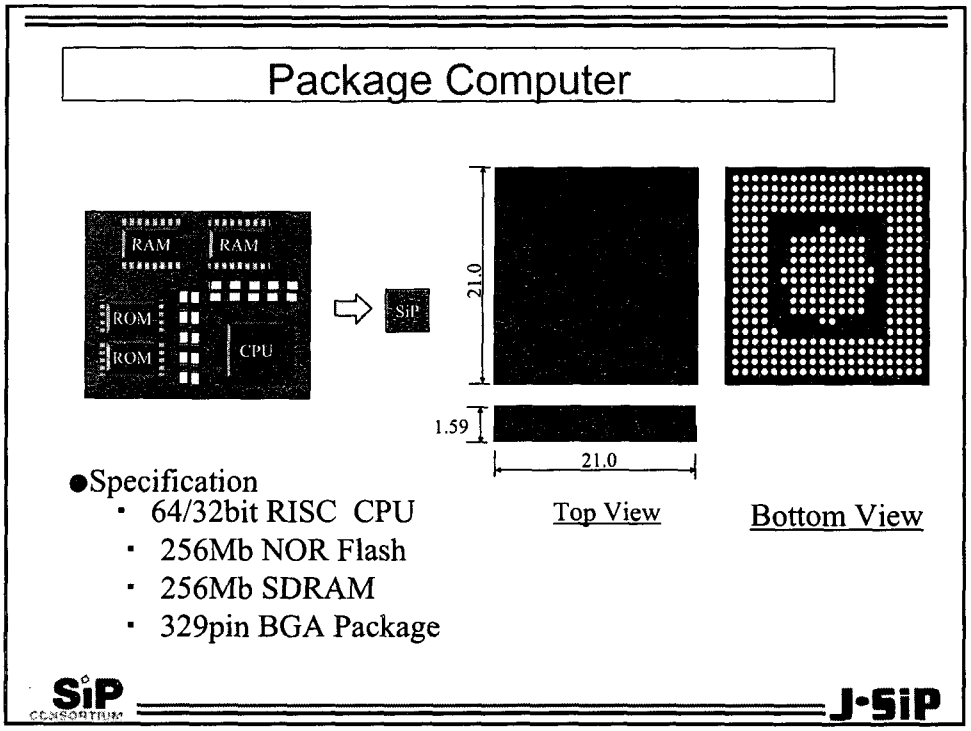
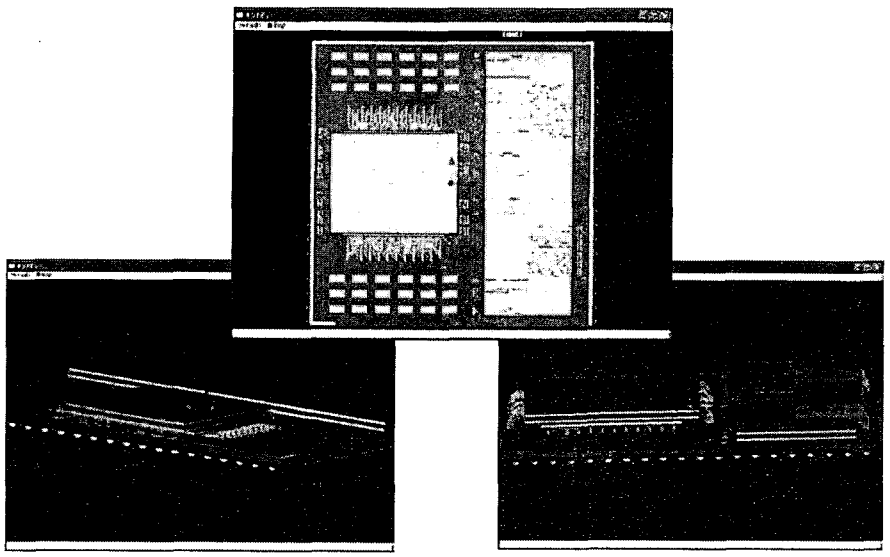
J-SiP


Package Computer
RAM
RAM
ROM
ROM
CPU
SiP
21.0
1.59
21.0
Top View
Bottom View
●Specification
· 64/32bit RISC CPU
· 256Mb NOR Flash
· 256Mb SDRAM
· 329pin BGA Package
SiP CONSORTIUM
J-SiP



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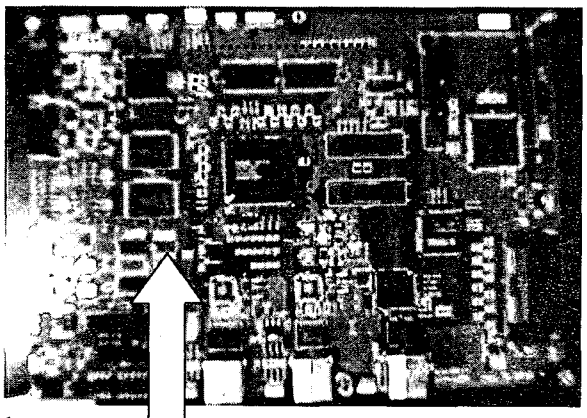
Robot System SiP Module



22.7cm

16.2cm

CPU + DRAM + Flash
+
Capacitor

WIND-SiP
5.0cm x 3.5cm

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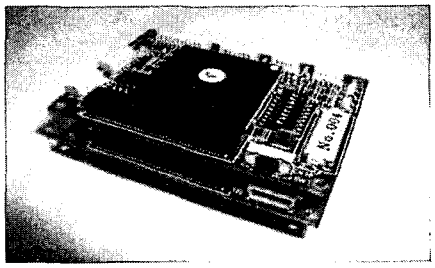
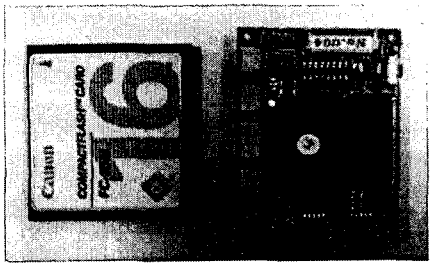
WIND SiP Module





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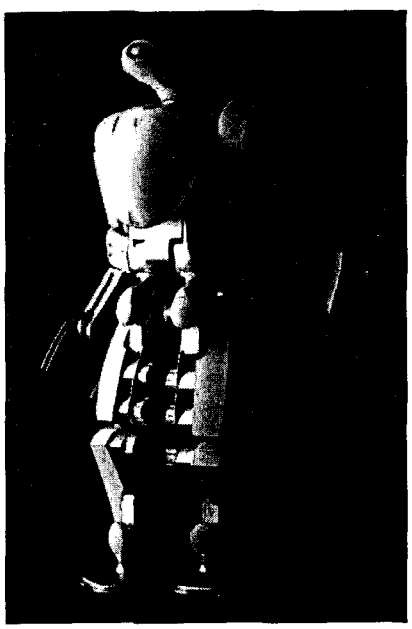

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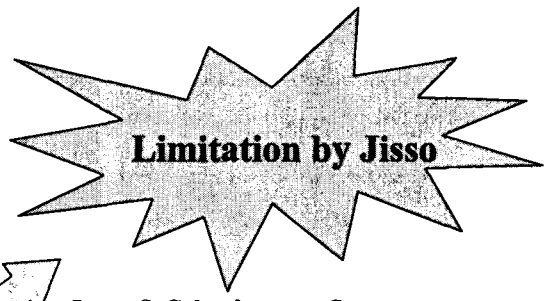
Limitation by Jisso Infrastructure



New Application

Customer Requests

(How to develop the New Products Quickly !)

- **Large SoC development Cost**
- **Long development TAT**
- **Large scale SOC can be applied on big number Production**
- **Limitation of high density assembly by 2D-Jisso**
- **SMT has no big differences in terms of the location (Japan or China) by Standardization**
- **Copy products are easily made**

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New Business Chance!

New 3D-Jisso Products

- **High Density Products Design**
- **3D-Jisso(All in One SiP)**
- **Within Passive Components**
- **Small and High Performance**
- **3D-Module**
- **Custom Products (Unique)**
- **Black box**
- **Very difficult to make Copy Products ! !**

Big Differences against 2D-Jisso (New Products)

3D-Jisso Design and Manufacturing Infrastructure

- **Passive component**
- **KGD Semiconductor Chip**
- **Manufacturing Service**

Customer Request

Quick Development

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You can reach J-SiP and SiP Consortium Web sight .

http://www.j-sip.co.jp

http://www.sip-c.com

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