마이크로스트립 선로를 이용한 GaAs-MMIC 제작공정 최적화

제이 프라카쉬 타쿠르†, 손창신† , 박준석†, 조홍구†, 김형석‡
국민대학교†, 중앙대학교‡

GaAs-MMIC Process Optimization Using Microstrip Line

J. P. Thakur†, Chang Sin Son†, Jun-Seok Park†, Hong-Goo Cho†, Hyeong-Seok Kim‡
School of Electrical and Electronics Engineering. Kookmin Univ†. & Chung-Ang Univ‡.

Abstract - This paper presents optimization of GaAs substrate thickness for GaAs-MMIC processes at high frequencies using a multidielectric microstrip line, that is fabricated using MMIC process

1. introduction

The growing popularity of microwave and millimeter wave communication systems demands compactness of the circuit modules with enhanced efficiencies of these systems. Monolithic Microwave Integrated Circuits (MMIC) satisfies these demands. However, progress in GaAs MMICs for frequencies up to 40 GHz and beyond depends almost entirely on the possibility of producing complex MMICs incorporating active components such as transistors as well as low loss passive microwave components like transmission lines and transmission line based components, lumped inductors, capacitors, etc. on a single chip [1, 2].

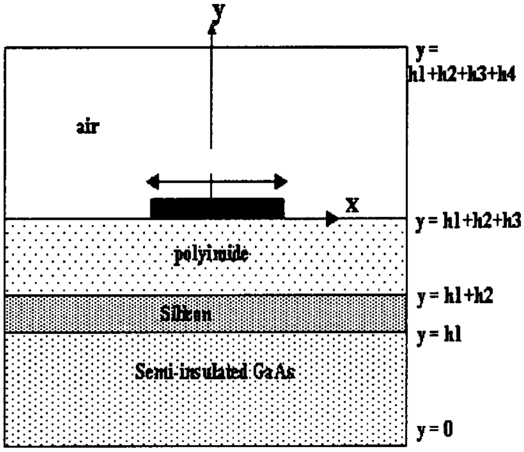

Figure 1. Cross-sectional geometry of multilayer microstrip line

In a GaAs MMIC process the Semi-insulated (SI) GaAs substrate thickness (3″ Wafer) chosen is typically 500-600 um. The wafer is thinned down from back side to 100-200 m after completion of the fabrication of MMICs. The handling of GaAs substrate becomes difficult once substrate is thinned down to 100-200 um as GaAs is a brittle material. The handling of GaAs substrate becomes a serious constraint if Via-hole processing is also needed, which is done using either RIE (reactive ion etching) or ICP (inductive coupled plasma). It is easy to etch a thin (100 um) substrate but difficult to handle. On the other hand a thick substrate is hard on the etching equipment but makes it easier to handle during subsequent processing. Another important consideration affecting the choice of substrate thickness is microwave losses. A thinner substrate is desirable to minimize the losses but handling become difficult and reverse is true for a thicker substrate. Hence accurate optimization of the substrate thickness is desired to cater to afore-mentioned considerations. This has been dealt with in the present paper.

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A single layer microstrip line is form by placing gate metal of active devices like MESFET (or HEMT) directly on a semi-insulating GaAs substrate. A multilayer microstrip line structure is fabricated by placing a silicon nitride layer (~0.7 um) directly on Semi- insulated GaAs substrate followed by a thick layer of polyimide (~1.18).

Many MMICs foundries use Silicon nitride (ε_r= 7.7) and Polyimide (ε_r=3.4) for fabricating high and low value capacitors. These layers also solve the purpose of passivating the surface of active devices like MESFET and HEMT. Thus it becomes necessary to model the effects of including these multiple layers on the electrical performance of the multilayer microstrip lines.

The present paper discusses the effect of substrate thickness and the frequency of operation on the electrical parameters of the single and multilayer microstrip lines, namely effective dielectric constant and characteristic impedance. Further, the study has been carried out to optimize the thickness of the GaAs substrate at different frequency ranges of operation. The computed results have been validated with the simulated results obtained from High Frequency Structure Simulator (HFSS), a FEM based software. This work is of importance for process optimization in GaAs MMICs foundries.

2.RESULTS AND DISCUSSION

GaAs Multilayer microstrip line has been fabricated on the GaAs substrate (ε_r = 12.9, tand δ = 0.0045) with layers of silicon nitride (ε_r = 7.7, h2 = 0.7μm, tand δ = 0) and polyimide (ε_r = 3.4, h3 = 0.18 μm, tand δ= 0) deposited on it [3].

At high operating frequencies such as 40 GHz, the wavelength is a few millimeters. Whereas a typical microstrip line thickness is approximately 2.5 μm which is at least 1000 times less than the wavelength. Hence the conductor thickness has been neglected in the analysis .

The variations of electrical parameters, namely effective dielectric constant, e_{eff} and characteristic impedance, Z_0, of the structure concerned have been studied as a function of height of the GaAs substrate, h_1, and the width of the strip, W at different frequency of operation. The study has also been carried out for single layer GaAs microstrip line.

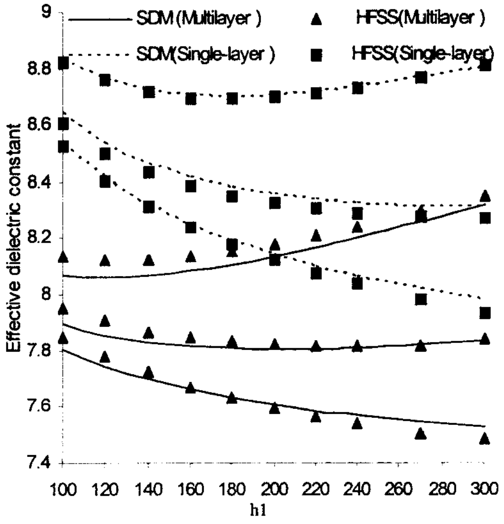

Fig. 2. Effective dielectric constant Vs GaAs Substrate thickness (h1) for w = 100 um at different frequency for Single-layer microstrip line

Fig. 2 and 3 show the variation of $_{eff}$ and Z_0 with h_1 at 1 GHz, 20 GHz and 40 GHz for W = 100 um.

R_1 $R_2$and show the range of thicknesses of the GaAs substrate that can be chosen at different frequency of operation. It has been observed in Figures that up to 150 um substrate thickness dispersion in characteristic parameters are around 3-5% but beyond this these are more dispersive, at 300 um thickness dispersion is around 10%. It is also observed that up to h_1 = 240 um, variation at 1 and 20 GHz is analogous and dispersion is limited to 3-4% but dispersive effects increases beyond h_1 = 240 um.

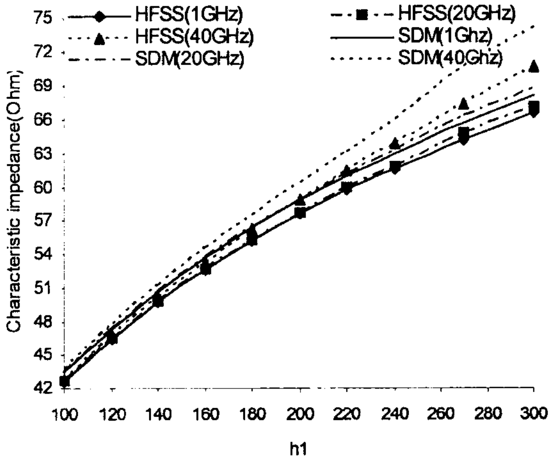

Fig. 3. Characteristic impedance Vs GaAs Substrate thickness(h1) for w = 100 um at different frequency for Single-layer microstrip line3

different frequency of operation. It is apparent form the figure that there is insignificant variation in Z_0 up to h_1 = 150 um at 1, 20 and 40 GHz but there is significant change in the values of Z_0 beyond h_1 = 240 m at frequencies beyond 20 GHz. Although the variation is significant for the thicknesses beyond h_1 = 150 um at frequencies higher than 20 GHz.

Hence the behavior of $_{eff}$ and Z_0 observed at for different frequencies with respect to substrate thickness infers that for the frequency range 1 to 20 GHz in designing of MMIC circuitsone can use substrate thickness in the range 100 to 240 m and for frequencies in the range 1 to 40 Ghz, 100 to 150 m substrate thickness can be used, which will lead to better performance of the circuit.

3. CONCLUSIONS

The above paper has presented a detailed parametric analysis of single layer and multilayer microstrip lines at different frequencies. crucial.

It has been shown that the dispersion behavior is similar in single and multilayer microstrip lines and the only difference lies in the magnitude of the ε_{eff} and Z_0. The study is expected to be useful for the GaAs foundry purposes by providing an efficient CAD approach for designing MMIC lines.

4. REFERENCES

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