2005년도 대한전기학회 하계학술대회 논문집 2005. 7. 18 - 20

Active Clamping 방식을 이용한 전력용 반도체의 최적 직렬연결 방법

김봉석, 고광철
대전력 응용공학 연구실, 한양대학교

Optimized Series Connection of Power Semiconductor Using Active Clamping Method

Kim Bong Seong, Ko Kwang Cheol
Applied High Power Engineering Lab, Hanyang University

Abstract - Power semicondcutor인 IGBT, MOSFET, GTO, SI-Thyristor등은 높은 스위치 신뢰성과 life time, 그리고 fast repetition rate 등을 지니고 있기때문에 medium/High voltage영역에서 스위치 사용이 대두되어 왔으나, Thyratron이나 Trigatron(Gap switch)와 비교하여 낮은 전압/전류를 스위칭하기 때문에 전통적으로 직렬연결을 통해 high voltage 영역의 스위치로 사용되어 왔다. 하지만, 직렬연결되어 있는 각각의 power semiconductor와 gate driving circuit의 on/off synchronization이 맞지 않기 때문에 부하의 급격한 변화에 따른 전압의 balance에 문제가 가장 심각하게 대두되어 왔다.
이러한 문제를 해결하기 위해서 gate driving circuit에서 제어를 해주는 방법과 power semiconductor에서 제어를 해주는 방법이 있으나 두 방식 모두 문제점이 있다.
본 논문에서는 기존의 zener clamping방식에서 벗어나 새로운 active clamping방식의 직렬연결을 제안했으며 시뮬레이션과 실험을 통해 나타난 이 결과들은 on/off transient 시 symmetry를 유지하는데 효과적이라는 것을 보여주고 있다.

1. Introduction

Thyratron and hard-tube switch are used typically for control of high voltage and high current at the field of the pulsed power and plasma applications.

In the case of designing and using hard-tube, pulse generator has wide range of impedance matching with better rectangular pulse shape, high duty cycle and long life time. It is needed the isolated driver and the additional power to control hard-tube with low efficiency due to high voltage drop.

Thyratron which is widely used for commercial high power switch, has good property of high di/dt, high peak current allowance with reliable performances. Thyratron, however, has also many drawbacks poor rectangularpulse shape generating, narrow impedance matching, and short life time [1].

There are presented to replace Thyratron and hard-tube switch to overcome these drawbacks, using power semiconductors such as IGBT, MOSFET, Thyristor, GTO, and etc,. There also have been proceeded many papers and academic researching to connect power semiconductor in series connect as high voltage switch since a decade.

Obviously, series connecting method of Power semiconductor has good advantages at the aspect of wide impedance matching, high duty cycle, good rectangular pulse shape generating with reliability.

However, it is still remained as significant trouble to keep voltage sharing balance of each power semiconductor at transient phase while switching.

There are proposed many control methods to keep voltage sharing balance at transient switching phase, especially from off state to onstate phase at series connected IGBT [2].

This paper will present steps of series connected IGBTs module design based on experimental data of typical series connection method that is used widely, and show steps of series connected IGBTs module that based on EMTP and new types of active collector-gate clamping method to hold synchronization at transient switching phase of IGBTs.

2. Experimental & Analytical Data of Pulse Generator using Series Connected IGBTS

2.1 Basic Experimental Data Acquisition

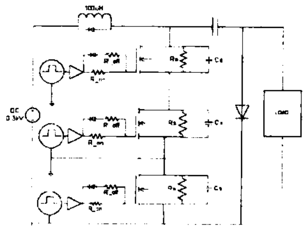

Figure. 1. Basic pulse generator circuit diagram and series connected IGBTs switch with auxiliary circuit to balance voltage sharing

For the first step, to find out influence on internal variables in IGBT and gate driver component that affect the switching phase symmetry at series connected IGBTs, typical series connected IGBTs switch is embodied as buck type negative pulse generator as shown Figure.1

Due to switching characteristics of series connected IGBT is quite different from single IGBT switching behavior, to calculate optimal R_g at gate driver, gate driving DC power requirement, and internal IGBT's capacitance components are necessary to be measured at the condition of IGBT in series connection [3].

These values are applied to simulate IGBT that are based on analytic model of MOSFET, like Figure 2.

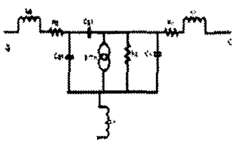

Figure 2. Analytical model of IGBT based on MOSFET mo del

Most of IGBT's parameters are found indirect calculation from IGBT's switching on/off waveform and time with gate driving waveform and datasheet.

These calculations are set to 1kV sharing at each IGBT and 10μs pulse generating condition with variable frequency as following equations of each switching phase in Figure 3. Table 1 indicates calculated internal circuit parameter of IGBT at the condition. [3] [4]

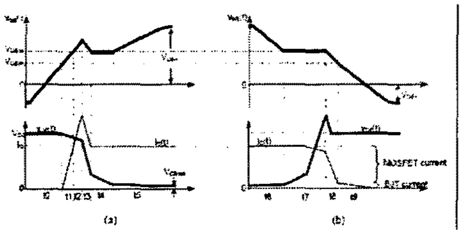

Figure 3. Switching waveform of IGBT (a) Turn on phase (b) Turn off phase

Ls calculation: $V_{L_s,effect} = L_s \times \frac{di_c}{dt}$, t2, t3 region

Cgc calculation: $V_{CE} = \frac{(V_{GG} - V_{GE,I_0})}{R_G \cdot C_{gc}}$, t4 region

Cres(reverse transfer capacitance, Cgc) calculation:

$$\frac{dV_{CE}}{dt} = \frac{V_{GE,I_0}}{C_{res} \cdot R_G}$$, t7 region

Cies(input capacitance, Cies=Cge+Cgc) calculation:

$$\frac{di_c}{dt} = g_m \frac{V_{GE,I_0}}{C_{ies} \cdot R_G}$$, t8 region

Table 1. Internal Circuit Parameters of IGBT in series connected, compared with single switching experiment. R_g was set to 1Ω.

Parameter	Single IGBT	IGBT in series connected	IGBT in Datasheet
C_{ies} ($C_{GC} + C_{GE}$) input capacitance	3700pF	2500pF	4000pF
C_{GC} gate-collector capacitance	250 pF	166 pF	300 pF

As auxiliary circuit components, Rs and Cs in Figure 1 are necessary to hold static and dynamic voltage balance. Rsconnected parallel to IGBT is necessary to prevent switch from being forced into avalanche at IGBT that has the lowest leakage current at steady state and Cs is needed not to be forced into voltage breakdown at the slowest IGBT among series connected. It is able to be altered Cs into RCD snubber or RC snubber circuit that depends on power semiconductor's switching property whether normally off or on switch state.

2.2 Asymmetry factors of Series Connected IGBTs of voltage equalization based on Experiment Data

Though transient or dynamic voltage equalization in series connection of power semiconductor is mentioned very simply at section A, it is very hard to obtain due to difference of IGBT that are connected in series, and different delay time of a gate driving output at each IGBT.

Figure 4-(a) shows 2kV switching output waveform of triple connected IGBT in series at terminal port of negative pulse generatorthat is used RCD snubber and C component in the condition of 10kHz operating frequency. Figure 4-(b) presents gate driving waveform at 2kV switching operation of IGBT switch. Though, most of oscillation factors that cause asymmetry of voltage balance stem from differences of gate drive circuit, over voltage stress is concentrated on high voltage side, IGBT side.

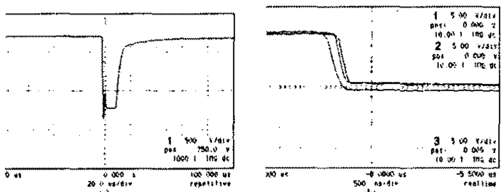

Figure 4-(a). Generated negative pulse with 50Ωdummy load
Figure 4-(b). Gate driving signal at the condition of Figure 4-(a)

2.3 Proposed Control Method and Circuit

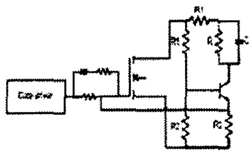

Figure 5. Proposed additional auxiliary circuit that is conne cted in parallel to IGBT

To diminish asymmetry of voltage balance, active voltage clamping at high voltage side is preferred. Figure 5 shows proposed additional active clamping circuit that consists of R, C, and transistor when it detects over voltage , C will compensate $C_{GC}$of IGBT that takes over voltage.

Operation of proposed auxiliary circuit is divided into 4 modes that depend on switching waveform of IGBT. Though, switching waveform mode of IGBT is divided into 9 modes as shown in Figure 3, imbalance of voltage sharing is observed at the phase of mode 2, 3 in Figure 3.

Thus, key point of symmetricvoltage balance at mode 2, 3 is achievedby equalizing input transfer capacitance, Cies by compensatingC_{GC}. Except different value of internal circuit value in IGBT and of delayed time in gate driver and gate signal oscillation, difference of external capacitance value also can be a factor of asymmetric voltage sharing. In experiment and simulation of proposed circuit, it is concentrated to transient phase of off switching in

IGBT and different delayed time and signal in gate driver.

Figure 6shows simulation data of proposed circuit while gate signal delay time is changed from 300ns to 1us that is based on basic experimental data at section A, and simulated waveform is executed under the condition of $200 \times e^{-9}$ seconds delay time. Simulation assumption is originated from gate driving delay time is dominant factor of asymmetric voltage sharing, and simulated output waveform is compared with parallel connected Rs and Cs components.

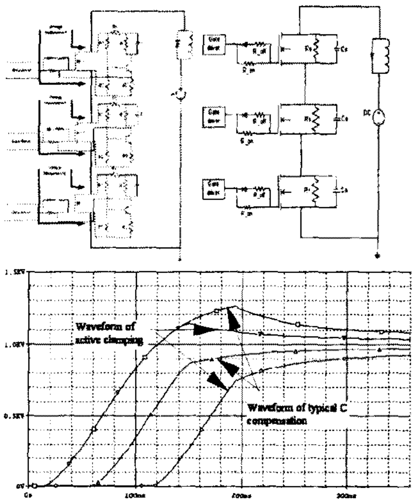

Figure 9. Simulation waveform of typical C compensation a nd proposed active clamping method

2.3 *Output Waveform of Proposed Circuit*

To verify output waveform of proposed circuit and method, verification is executed at the same condition of basic experiment, operating frequency is varying from 1Hz to 10kHz, pulse width is fixed at 10us.

There have two advantages of proposed circuit even in comparison of existing active clamping method. Rs, compensating resistor that is connected in IGBT for static voltage balance at on or off steady state of IGBT switch is selected to flow two or three times of leakage current in IGBT. At the proposed circuit, R1 value is able to be selected as two times of Rs at typical connection method to diminish energy loss of high side.

The other strong point is not to be needed additional calculation of snubber capacitance at the proportion to varying operating frequency at typical connection method, because C in auxiliary circuit compensates C_{CG} from on state to off state transition at the phase of mode 2, 3 in Figure 3.

Most of current active clamping methods are consist of zener diode that detect expected over voltage with Capacitor to compensate C_{CG}.[5] Internal capacitance of he zener diode also can be a serious oscillation factor to hold high voltage zener breakdown voltage at series connected IGBT switch and cause much energy loss compared with proposed active clamping method.

It is necessary needed to calculate amount of charge compensating at C_{CG} in IGBT, due to being transferred charge from IGBT side to gate side must also be a serious oscillation or distorted waveform.

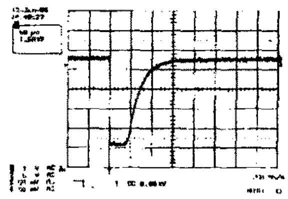

Figure 10. Switching waveform of series connected IGBT with proposed circuit at the condition of 1kHz operation frequency, at $50\mu s$ pulse width at terminal 5kV output of negative pulse generator.

3. 결 론

In this paper, there are performed two kinds of approach to design and improve negative pulse generator for WIPS (Wire Ion Plasma Source) both experiment and simulation.

Active clamping method of IGBT in series connection to synchronize voltage sharing at transient switching time shows improved result, compared to typical series connection method of IGBT. In proposed circuit, amount of being transferred charge to gate diver side have to be measured and calculated very carefully to design auxiliary circuit because it can cause oscillation waveform in gate driving waveform.

[참 고 문 헌]

[1] D.M.Goebel, R. J. Adler, D. F. Beals, and W. A. Reass, "Handbook of plasma Immersion Ion Implementation and Deposition," 10th IEEE International Pulsed Power Conf., 1995, pp.1243-1248

[2] Palmer, P.R. Githiari, A.N. Leedham, R.J "A comparison of IGBT technologies for use in the series connection," Power Electronics and Variable Speed Drives, 1996. Sixth International Conference on (Conf. Publ.No.429) 23-25 Sept. 1996 Page(s):236 - 241

[3] Brambilla, A.; Dallago, E.; Romano, R.; "Analysis of an IGBT power module," Industrial Electronics, Control and Instrumentation, IECON '94., 20th International Conference on Vol.1, 5-9 Sept. 1994 Page(s):129 - 134

[4] Ju Won Baek, Dong-Wook Yoo, and Heung-Geun Kim, "High-voltage switch using series-connected IGBTs with simple auxiliary circuit," Industry Applications, IEEE Transactions on Vol 37, Issue 6, Nov-Dec 2001 Page(s):1832 - 1839

[5] Soonwook Hong and Yong-Geun Lee, " Active gate control strategy of series connected IGBTs for high power PWM inverter," Power Electronics and Drive Systems, 1999. Vol.2, Page(s):646 · 652