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저전력 분야 응용을 위한 32 nm 금속 게이트 전극 MOSFET 소자의 게이트 workfunction 의 최적화

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Gate Workfunction Optimization of a 32 nm Metal Gate MOSFET for Low Power Applications

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Abstract - The feasibility of a midgap metal gate is investigated for 32 nm MOSFET low power applications. The midgap metal gate MOSFET is found to deliver a driving current as high as a bandedge gate one for the low power applications if a proper retrograde channel is used. An adequate design of the retrograde channel is essential to achieve the performance requirement given in ITRS roadmap. In addition, a process simulation is run using halo implants and thermal processes to evaluate the feasibility of the necessary retrograde profile in manufacturing environments. From the thermal budget point of view, the bandedge metal gate MOSFET is more vulnerable to the following thermal process than the midgap metal gate MOSFET since it requires a steeper retrograde doping profile. Based on the results, a guideline for the gate workfunction and the channel profile in the 32 nm MOSFET is proposed.

I. Introduction

A metal gates has been suggested in the ITRS roadmap to eliminate the adverse effect of poly depletion, boron penetration and high poly sheet resistance [1]. In selecting the gate metal material, the workfunction of the metal gate should be the most considered since it determines the threshold voltage of the MOSFET. A bandedge metal gate has been believed to be the optimal choice for sub-50 nm high performance applications(about 4.2 eV for NMOS and 5.1 eV for PMOS) [2,3]. However, when CMOSFET is integrated, use of the bandedge metal gate will make the fabrication process complicated and expensive. To improve the manufacturability of the bandedge metal gate MOSFET, various integration schemes have been reported, but yet offer a simple solution. In this work, the effect of the metal gate workfunction on the MOSFET performance is studied for the low stand-by power applications, which requires a very low I_{off}. The device performance of a midgap metal gate MOSFET is compared against one of the bandedge using TCAD simulation. In addition, the feasibility of the channel doping profile required for each workfunction is studied at various thermal budgets.

II. Simulation methodology

A commercial device simulator ATLAS and process simulator ATHENA from SILVACO have been used for this work. Classical drift and diffusion model have been used. For carrier mobility, field and concentration dependent models are used. Details of MOSFET studied here are assumed based on ITRS roadmap [1]. The equivalent oxide thickness of gate dielectric is 1.5 nm. It is assumed that Source/Drain (S/D) junction depth is 18 nm and S/D extension junction depth is 8.8 nm. The doping concentrations of S/D and S/D extension are $2.0\times10^{20}cm^{-3}$ and $8.0\times10^{19}cm^{-3}$ respectively. The nominal gate length is 32 nm and ±4 nm gate CD variation is considered (identified as L_-, L_{nom} and L_+ respectively). Supply voltage of 1.1V is used.

III. Results and Discussions

To meet I_{off} = 300 pA/μm at L_- devices, substrate doping concentrations are calculated for various gate workfunction in Fig.1.

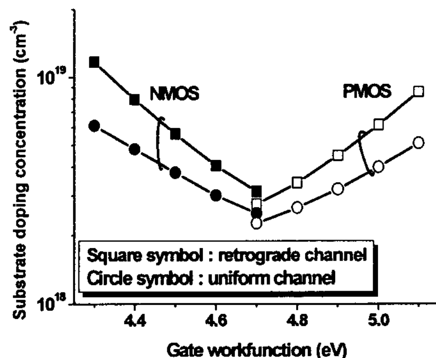

Fig.1. Substrate doping concentration to meet a given I_{off} for L_- devices.

In Fig.1, a retrograde channel is also considered and it consists of a 5 nm-deep lightly doped ($1.0\times10^{16}cm^{-3}$) region under which the high doped substrate lies. For MOSFET performance comparison, I_{on} at L_g = 36 nm and L_g = 28 nm are calculated as shown Fig.2. It is shown that the use of retrograde channel can enable to improve I_{on} for midgap gate MOSFET by taking advantage of high mobility and suppressed short channel effect.

Note in Fig.2, the retrograde channel devices have higher I_{on} than the uniform channel devices at both NMOS and PMOS. I_{on} of the midgap (Φ_m =4.6 eV

and 4.7 eV for NMOS and Φ_m = 4.7 eV and 4.8 eV for PMOS) gate device with the retrograde channel is comparable to one of the optimum workfunction (Φ_m = 4.4 eV for NMOS and Φ_m = 5.0 eV for PMOS) gate device with the uniform channel.

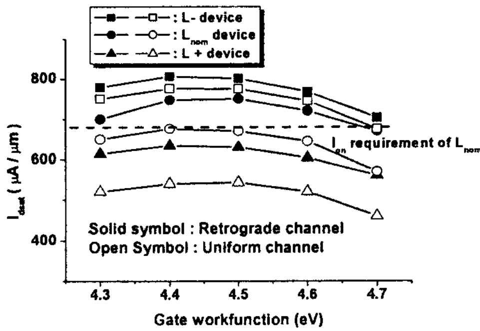

Fig.2(a). Comparison I_{on} of NMOS with uniform channel and retrograde channel at V_{gs}=V_{ds}=Vcc. The dash line indicates I_{on} requirement of ITRS at L_{nom}

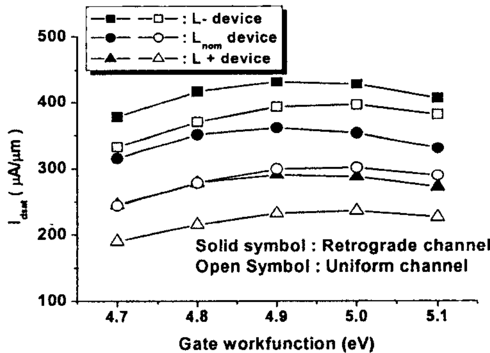

Fig.2(b). Comparison I_{on} of PMOS with uniform channel and retrograde channel at V_{gs}=V_{ds}=Vcc.

In SiO_2 based gate dielectric transistors, a super-steep retrograde channel has been known unpractical due to high temperature gate oxidation process and S/D activation process. However, an alternative gate dielectric materials such as HfO_2 will likely replace the oxide gate dielectric in the sub-50 nm CMOS process for the suppression of the gate leakage current. The use of the alternative gate dielectric materials is expected to maintain implanted retrograde channel even after the gate dielectric formation because of its low temperature process (under 550°C) [4-6]. RTA spike annealing for S/D activation and low temperature side wall formation process [7,8] are also expected to diffuse dopants insignificantly. Considering the usable processes and heavy implanted species, such as indium the necessary retrograde channel will be likely obtained for 32 nm low power applications.

To investigate the feasibility of the retrograde channel, process simulation has been performed. Indium and arsenic have been used for the retrograde channel and the S/D implants, respectively. Shown in Fig.3 is the substrate implant dose, required to meet I_{off} = 300 pA/μm at L= L- with various gate workfunctions and anneal times.

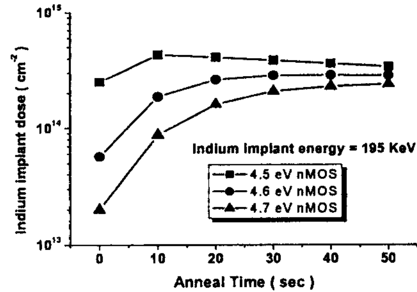

Fig.3. Required indium implant dose to meet I_{off} = 300 pA/μm for L with annealing at 1000°C

As the anneal time increases, the required substrate implant dose increases in order to suppress short channel effect. Note that the necessary implant dose for the midgap device rises more rapidly than one for the bandedge one because the lateral diffusion of the same S/D has to be suppressed. Using the implant condition above, I_{on} and threshold voltage V_{th} are simulated as the anneal time increases (Fig.4 and Fig.5). It is observed that I_{on} degrades more in the bandedge device than the midgap one as the anneal time increases. It is believed that the necessary steep profile can not be kept in the longer annealing, causing the performance loss.

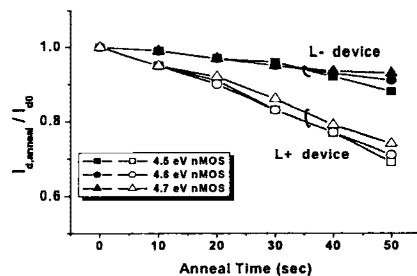

Fig.4. I_{on} comparison between L device and L- device using implant dose in Fig.3. I_{d0} is saturation current without anneal.

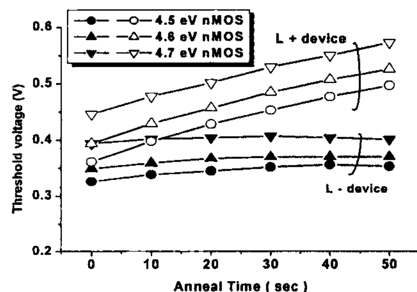

Fig.5. Threshold voltage (V_T) comparison between L device and L device using the implant dose shown in Fig.3.

As shown in Fig.4. I_{on} of L_{-} device decreases more dramatically in 4.5 eV than in 4.7 eV. For 4.5 eV metal gate, the annealing process results in a high surface doping concentration and it causes a lower carrier mobility and large V_T roll-off. Based on the results, it is believed that the bandedge gate device is more vulnerable to the subsequent thermal process than the midgap gate one.

Fig. 6 shows band-to-band tunneling leakage current for I_{off}. For a given I_{off} requirement, I_{source} and $I_{substrate}$ is calculated as the S/D extension doping increases. As shown earlier, the midgap device has less substrate doping, resulting in less BTB tunneling current than the bandedge one. Note that the I_{off} requirement can not be met in the 4.5 eV device when the extension doping increases beyond 7×10^{19} cm^{-3}. Considering the trend of higher doping concentration in the extensions, this result implies the extension design of the bandedge gate will be more limited.

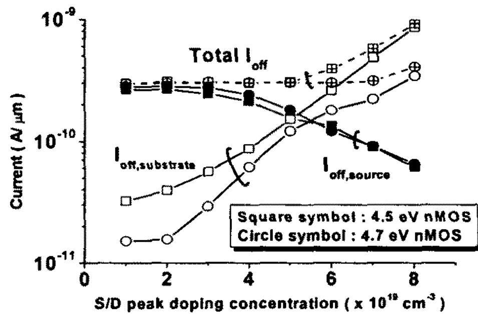

Fig.6. I_{off} band-to-band tunneling current and source current in the midgap and bandedge devices.

IV. Conclusion

In the foregoing discussions, it is found that the midgap metal gate device can be considered as the gate electrode for the low power applications when a proper steep retrograde channel is used. From the thermal budget point of view, the midgap device is preferred over the bandedge one since a steeper retorgrade profile is required in the bandedge device. Nonetheless, it is suggested that the thermal processes should be tightly controlled in order to maintain the retrograde channel profile. In addition, the midgap metal gate devices has more S/D design margin as the band-to-band tunneling leakage becomes a dominant I_{off} leakage mechanism, which is a valid assumption in sub-50 nm CMOS technology.

Acknowledgement

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