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Investigation of thermal stability of strained Si on relaxed SiGe layer

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MOSFET device utilizing a strained-Si channel on relaxed SiGe buffer layer is one of the most promising structurefor the next-generation CMOS integration scheme below 50 nm technology node because of enhanced channel mobility and compatibility with conventional Si CMOS processes. For the practical adoption of strained-Si channels into nano-CMOS technology, fabrication methods of strained-Si/relaxed SiGe/Si structures and their compatibility with post-thermal processes are to be obtained. In particular, stability of strained-Si channels on relaxed SiGe layers is of great concern because formation of misfit and threading dislocations and increase of surface roughness can occur during elevated temperature processing due to thermal-induced instability of strained-Si layers. In this study, we investigated thermal stability of strained-Si on relaxed SiGe layerat elevated RTA (rapid thermal annealing) temperatures. Strained-Si channel layers on the relaxed Si1-xGex(x=0.2) buffer layer were deposited by reduced-pressure chemical vapor deposition (RP-CVD). In order to investigate the thermal stability of fabricated strained-Si/relaxed-SiGe/Si(001), RTA treatments were carried out at the temperature range of 700~950℃ in N_2 ambient for 60sec.