A CMOS-based Electronically Tunable Capacitance Multipliers

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Abstract: A CMOS-based Electronically Tunable Capacitance Multipliers, which can be magnified the value of a grounded unit capacitance, is presented in this article. The multiplication factor is varied by the ratio of the bias currents. The proposed circuit is simple, small in size and suitable for implementing in standard CMOS process. PSPICE simulation results demonstrating the characteristics of the proposed circuit are included.

Keywords: Capacitance multiplier, voltage follower, current multiplier, low-voltage.

1. INTRODUCTION

Some real-time applications such as integrated lock-in amplifiers, sampled-data systems, and capacitive sensor interfaces, they often require the implementation of the high capacitive values for the long time constants [1]-[3]. In a standard CMOS process, the parallel-plate capacitors are implemented by two polysilicon layers. A typical specific capacitive value is about 1fF/μm^2 [4]. This means that a large silicon area of about 0.1mm^2 is necessary to obtain 100pF in capacitance value.

Nowadays, the complex electronic circuits are being integrated on the same chip. The chip area minimization is the one of the most problems to be solved. Accordingly, they have been much effort to reduce the silicon area for high capacitance values realization using the capacitance multiplication topology [4]-[6].

The classical approach is based on the use of two operational transconductance amplifiers (OTAs), an operational amplifier (op-amp), and a grounded capacitor [5] to realize the capacitance multiplier. The frequency performance achieved by this approach is limited by the narrow bandwidth of the op-amp topology. Moreover, this approach requires the high supply voltage. Alternatively, an approach in literature [4] is realized using the second-generation current conveyor (CCII) and two resistors to obtain the high capacitance gain factors. The limitation of this approach is due to the characteristic of two resistors, which unsuitable for implementing in monolithic integrated circuit form. In addition, the CMOS based approach with simple circuit configuration [6] provides wide dynamic range and very low power dissipation. However, the multiplication factor based on the on-chip tuning technique of this approach is depended on the gain of current mirrors.

The purpose of this paper is to present the electronically tunable capacitance multiplier. The realization method is suitable for fabrication using CMOS technology. The proposed capacitance multiplier comprises the voltage follower and the current multiplier with low voltage operation. The basic performances of the proposed circuit are confirmed by PSPICE analog simulation program.

2. CIRCUIT DESCRIPTION
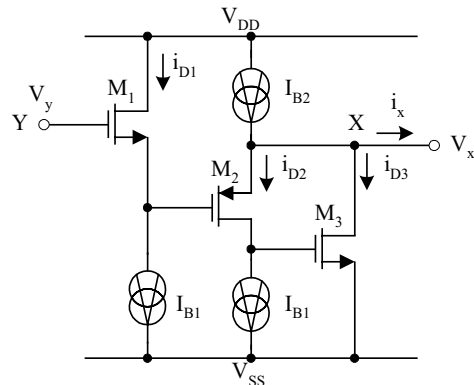
2.1 Voltage follower

Fig. 1 Voltage follower circuit

Figure 1 shows the voltage follower circuit that the relationship between the voltage at port Y and port X can be written by

$$V_y = V_{GS1} - V_{GS2} + V_x \qquad (1)$$

All transistors are operated in their saturation regions. The drain current of transistor operated in saturation region is expressed as

$$i_D = \frac{\mu C_{ox} W}{2L}(V_{GS} - V_T)^2 = K(V_{GS} - V_T)^2 \qquad (2)$$

where K, V_{GS} and V_T are the device transconductance parameter, the gate-to-source voltage and the threshold voltage, respectively.

In the BSIM MOS model of the 0.5μm CMOS process, K of NMOS (K_n) is larger than K of PMOS (K_p) about 3.9. Hence, we design the ratio of channel widths and lengths (W/L) of M_2 larger than M_1 about 3.9 and the drain current of M_1 and M_2 are equals that can be written as

$$K_n = 3.9K_p \qquad (3)$$

$$i_{D1} = i_{D2} = I_{B1} \qquad (4)$$

The gate-to-source voltage of transistors M_1 and M_2 are equal or
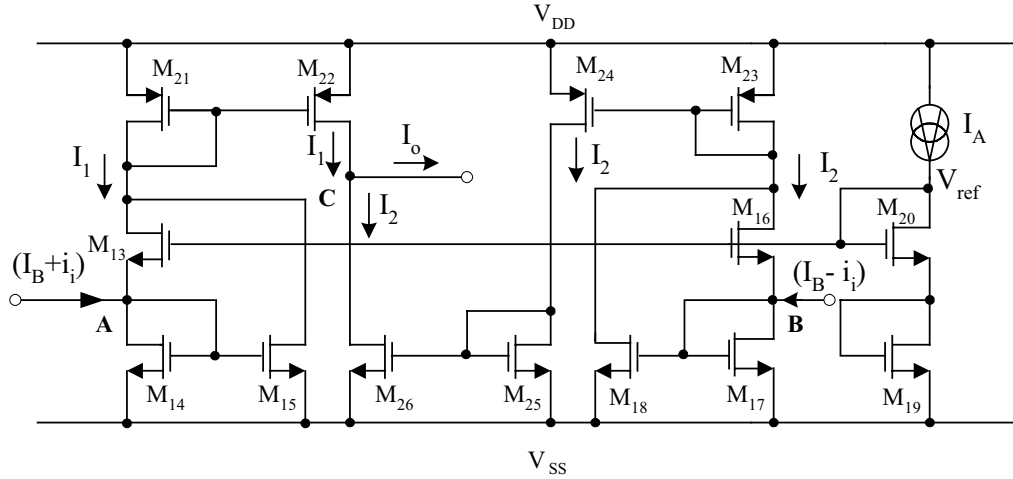
$$V_{GS1} = V_{GS2} \qquad (5)$$

Fig. 2 Current multiplier circuit

Then port X voltage is forced to equal that of port Y,

$$V_x = V_y \qquad (6)$$

the transistor M_3 and the current source I_{B2} form the negative feedback loop to reduce the resistance at port X. The current source I_{B2} can be written as

$$I_{B2} = I_{B1} + i_x + i_{D3} \qquad (7)$$

Hence, The resistance at port X of the circuit in figure 1 that can be expressed as

$$r_x \approx \frac{1}{g_{m2}g_{m3}r_{l1}} \qquad (8)$$

2.2 Current multiplier

The current multiplier circuit [7] is shown in figure 2. Groups of transistors (M_{13}, M_{14} and M_{15}) and (M_{16}, M_{17} and M_{18}) function as current-squaring circuits, where port A and B are input ports. Transistors M_{19}, M_{20} and the current source I_A supplies the bias voltage V_{ref} to M_{13} and M_{16}. Let us assume that all transistors in the circuit are characterized by the square-law model of MOS transistor operating in the saturation region. All the transistors, except M_{22} and M_{24}, have the same aspect ratio W/L. If the differential input currents, (I_B+i_i) and (I_B-i_i), where i_i is a small signal current, flow into ports A and B, respectively. Currents I_1 and I_2 can be expressed as

$$I_1 = 2I_A + (I_B + i_i)^2/(8I_A) \qquad (9)$$

$$I_2 = 2I_A + (I_B - i_i)^2/(8I_A) \qquad (10)$$

Where, the current $|I_B| + |i_i| \leq 4I_A$. to keep all devices in the on state. These currents are multiplied n times by the current mirrors formed by (M_{21} and M_{22}) and (M_{23} and M_{24}) where $(W/L)_{M21}(W/L)_{M22} = (W/L)_{M23}(W/L)_{M24} = n$. Because M_{25} and M_{26} function as a unity gain current mirror, from eqns. 9 and 10, the output current can be written as

$$i_o = n(I_1 - I_2) = ki_i = (nI_B/2I_A)i_i \qquad (11)$$

where, i_o flows out at port C. We can see that the small signal current is amplified by the factor k and this factor can be varied electronically.

2.3 Proposed circuit

The proposed CMOS-based Electronically Tunable Capacitance Multipliers is shown in figure 3. In this circuit, the transistors M_5, M_6 and M_7 are the current mirror that reflect the drain current of the transistor M_4 (i_{D4}) to port D and E, respectively. The current i'_i is equal to $i_{D4} - I_{B3}$ that flow in the opposite direction of the current i_i. The circuit operation can be explained as follow. The input signal voltage v_{in} is applied and the current i_i is equal to

$$i_i = v_{in}sC_{ext} \qquad (12)$$

The current i_i is amplified by the current multiplier formed by M_{14} to M_{26}. The amplified current i_{ext} can be written as

$$i_{Cext} = (nI_B/2I_A)i_i = ki_i \qquad (13)$$

Thus the relationship of the input voltage v_{in} and the current $i_{in} = i_{Cext}$ can be expressed as

$$i_{in} = skC_{ext}v_{in} \qquad (14)$$

or

$$C_{EQ} = kC_{ext} = (nI_B/2I_A)C_{ext} \qquad (15)$$

Where C_{EQ} denotes the equivalent capacitance at input mode.

3. SIMULATION RESULTS

The performances of the proposed circuit were studied by using PSPICE analog simulation program. The BSIM MOS model of the 0.5µm CMOS process was used in the circuit simulation. The ratio of channel width and length (W/L) of the devices are shown in Table 1. The supply voltage $V_{DD} = -V_{SS} = 1.5V$. The current source I_{B1}, I_{B2} and I_{B3} are set to 10µA, 60µA and 50µA, respectively.

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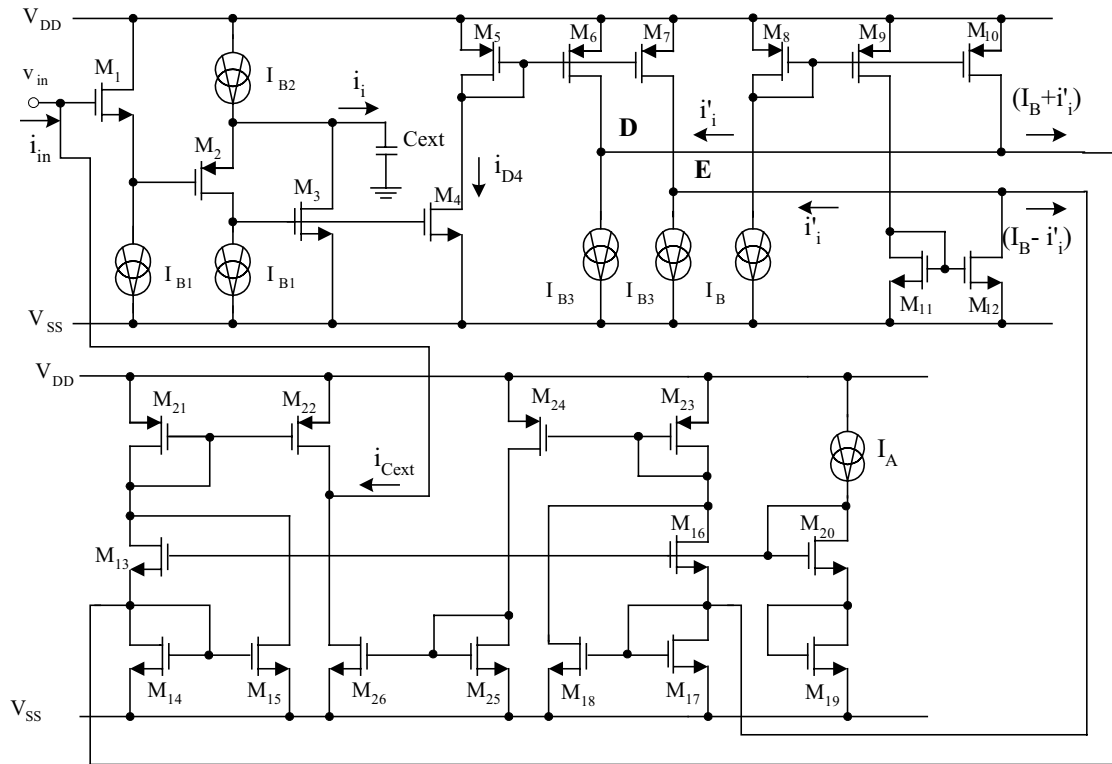
Fig. 3 Proposed circuit

Table 1 The ratio of channel widths and lengths

Device	W/L(μm)
M_1	8/1
M_2	31.5/1
M_3, M_4	32/1
M_5 - M_{21}, M_{23}, M_{25}, M_{26}	40/1
M_{22}, M_{24}	n(40/1)

Figure 4 shows the simulated equivalent capacitance. The error from the expected value is shown in figure 5. The bandwidth of about 274MHz is observed as shown in figure 6.
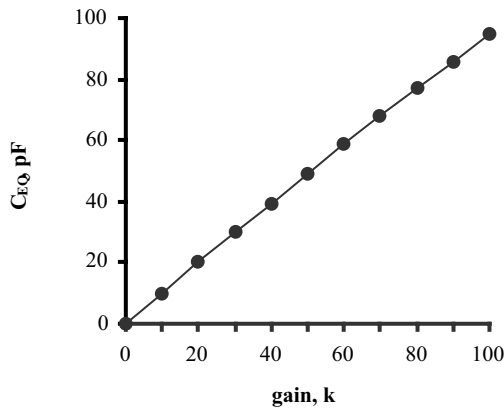

Fig. 5 Percentage error of C_{EQ}

Fig. 4 Variation of the equivalent capacitance C_{EQ} with gain k
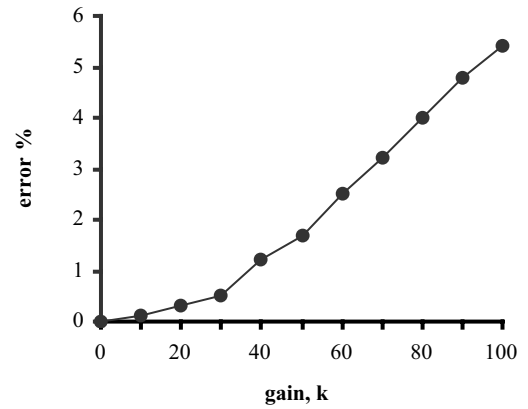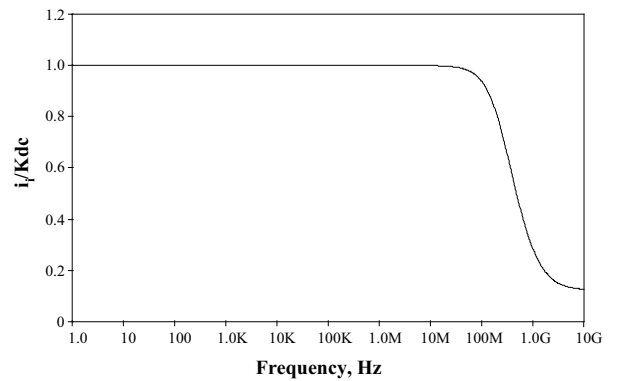

Fig. 6 Frequency response

4. CONCLUSION

This paper describes electronically tunable capacitance multiplier, which is varied by the ratio of the bias currents. The circuit configuration is simple and small in size. The realization method is suitable for fabrication using standard CMOS process. The transfer characteristic and frequency response of the proposed circuit are included.

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